SH7760 Solution Engine2

Overview

(MS7760CP01P)

1st Edition

Hitachi ULSI Systems Co., Ltd.

MS7760CP01P-M

[Notice]

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Notes on Using the MS7760CP01P

Thank you for your purchasing our MS7760CP01P board (simply called Solution Engine2 in this manual). Read the following notes and cautions before using Solution Engine2.

Solution Engine2 Components

Confirm that the following components are all contained after unpacking.

Product model: MS7760CP01P

- Solution Engine2 main unit (CPU board, LCD board, debug board and I/O board)
- AC adapter
- RS-232C cable
- CD-ROM (Software, Solution Engine2 User's Manual (This Manual))
- Big-endian monitor EPROM
- Software License Agreement
- User Registration Card

Safety Instructions

• Read this page carefully and keep in mind the instructions before using T-Engine.

CAUTION If ignored, there is a risk of death or heavy injury.

WARNING If ignored, there is a risk of injury or equipment damage.

CAUTION

• If smoke or abnormal smell arises from the board, stop using Solution Engine2, disconnect the AC adapter immediately from the receptacle and turn off Solution Engine2.

• Don’t disassemble or modify Solution Engien2 to avoid a risk of high-voltage electric shock or fire.

• Don’t drop water or liquids onto Solution Engine2 to avoid a risk of electric shock or fire. When water or liquid is dropped onto the board, disconnect the AC adapter immediately from the receptacle, and wipe it with a soft cloth to avoid a risk of electric shock or fire.

• Don’t fall objects (line or solder scrap) onto Solution Engine2. If an object is dropped into it, disconnect the AC adapter immediately from the receptacle, turn off Solution Emgine2, and remove the object from the inside of the board to avoid a risk of electric shock or fire.

• Use a dedicated AC adapter that comes standard with Solution Engine2 to avoid a risk of electric shock, abnormal heat or fire.

• Don’t use inflammable liquids (alcohol, benzine or thinner) for cleaning the board to avoid a risk of fire.

• Don’t place a heavy item on the AC adapter cord. To avoid a risk of electric leakage, fire or electric shock, don’t allow the AC adapter cord to be damaged or modified.

• Don’t unplug the AC adapter cord with wet hand to avoid a risk of electric shock. When unplugging the cord, grasp and pull the plug instead of the cord. Don't pull the AC adapter cord to avoid a risk of cord damage, electric shock or fire.

• Don’t use the packaged AC adapter (that comes standard with Solution Engine2) for other equipment to avoid a risk of electric shock, abnormal heat or fire.

• To power an external device from Solution Engine2's internal power supply, don’t supply a current over the permissible level of each power supply. If the supplied current exceeds the permissible current level, there is a risk of electric shock, abnormal heat or fire.

WARNING

• When Solution Engine2 is powered and used for a long time, it may be heated up to a temperature of about 50ºC. Though this is not a fault with Solution Engine2, there is a risk of low-temperature burn injury if skin touches it for a long time.

• Don’t use or store Solution Engine2 in a place subject to direct sunlight or near the heater to prevent Solution Engine2 from being deformed due to heat.

• Don’t store Solution Engine2 in a dusty or humid place.

• Turn off the power before connecting cables or equipment. When this caution is ignored, a fault may occur with Solution Engine2.

• When connecting the AC adapter to the receptacle, check the polarity and connection beforehand to avoid a risk of electric shock, fire or fault.

• Don’t distribute or permit the use of Solution Engine2 to those who may use it for purposes that may disturb or threaten international peace or security and don’t use it by yourself for malicious purposes. When exporting the purchased Solution Engine2, observe the foreign exchange law and take appropriate action.

Guarantee

• The system is repaired for free within a period of guarantee (one year after delivery) so long as it is used under normal conditions (normal environmental conditions, normal usage). The following lists the cases where Solution Engine2 must be repaired for value regardless of the period of free guarantee.

- System malfunctions due to natural disasters.
- System modification by users
- System malfunction due to incorrect use

• Solution Engin2 is specifically designed to serve various evaluation purposes prior to product development. Don't incorporate it into the product itself. We do not guarantee the performance of Solution Engine2 when used inside a product.

Others

• The product names in this manual are trademarks or registered trademarks of the respective manufacturers.

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1. System Configuration

1.1 Solution Engine2 Features

The following summarizes the main features of Solution Engine2.

(1) The manual covers all information about Solution Engine2, including the circuit diagrams, connector specifications and internal logic of FPGA employed on this board.

(2) The peripheral LSI chips (PCMCIA controller and sound generator chips) are commercially available.

(3) This board contains the PCMCIA controller, sound generator chip, SIM card connector, etc., so that application systems can be developed taking advantage of them.

(4) This board contains two SH7760 buses (address bus and data bus) and one extension slot subject to control signal output so that users can connect user-specific hardware.

1.2 Solution Engine2 Configuration

Figure 1.1 shows a Solution Engine2 system configuration and Figure 1.2 a Solution Engine2 block diagram. Besides Solution Engine2 and its accessories, prepare any user-specific devices as needed.

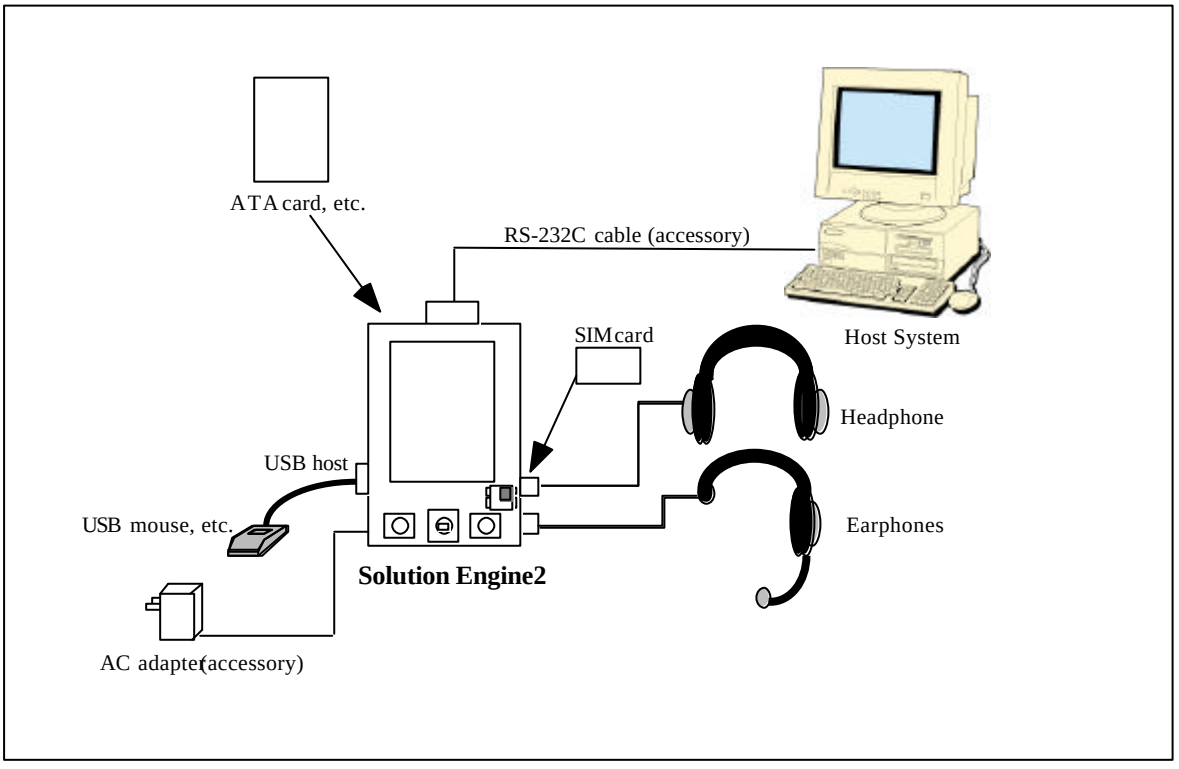


Figure 1.1 Solution Engine2 System Configuration

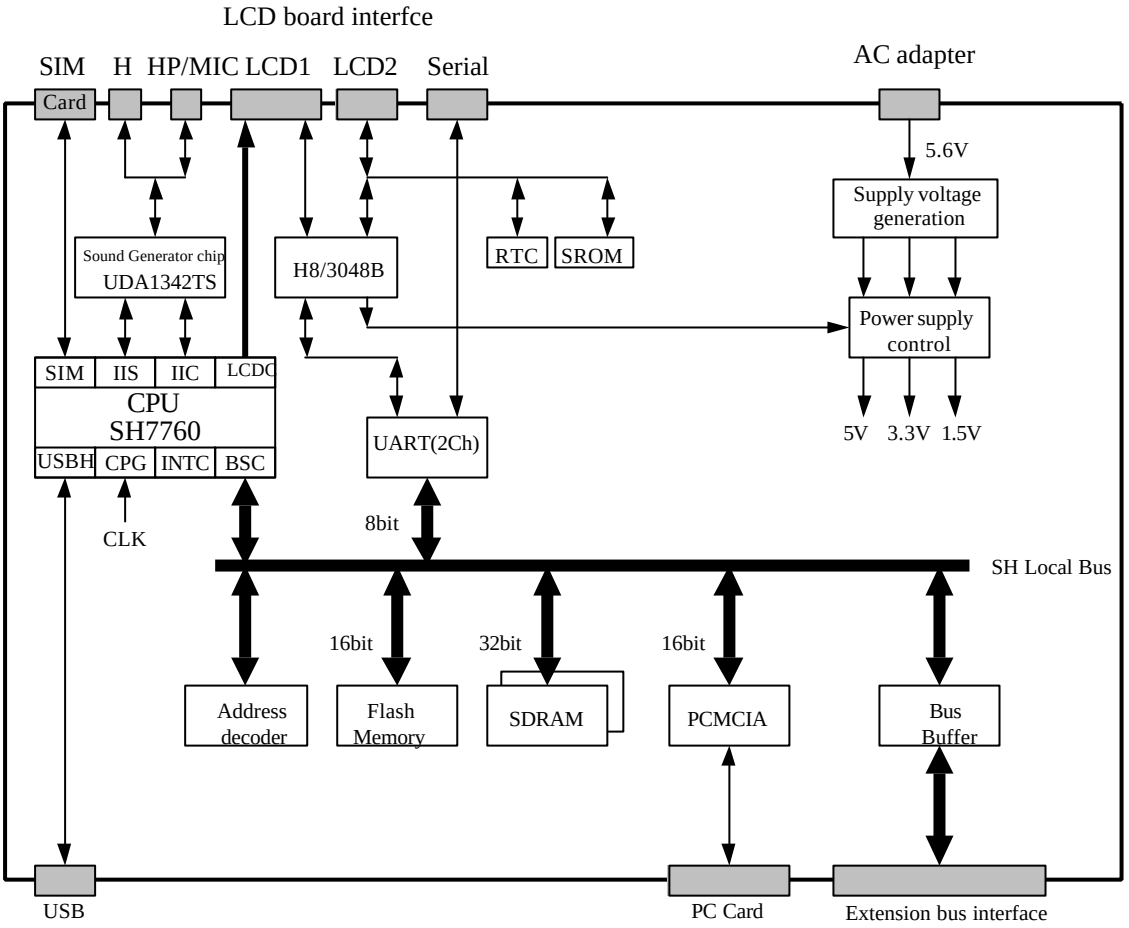


Figure.1.2 Solution Engine2 Appearance

1.3 Solution Engine2 Appearance

Solution Engine2 consists of four boards: CPU, LCD, debug and I/O. Figure 1.3 is an external view of the Solution Engine2. Figures 1.4 to 1.7 show the appearances of the respective boards (CPU, LCD, debug and I/O boards).

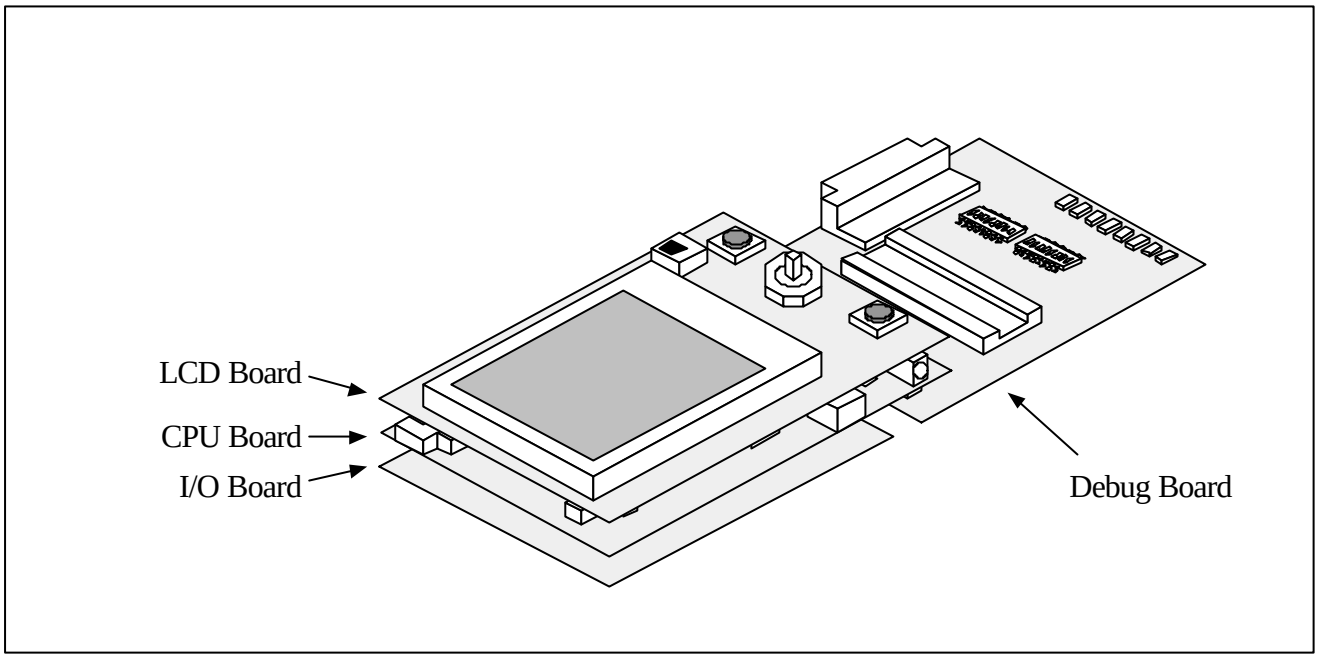


Figure.1.3 Solution Engine-External View

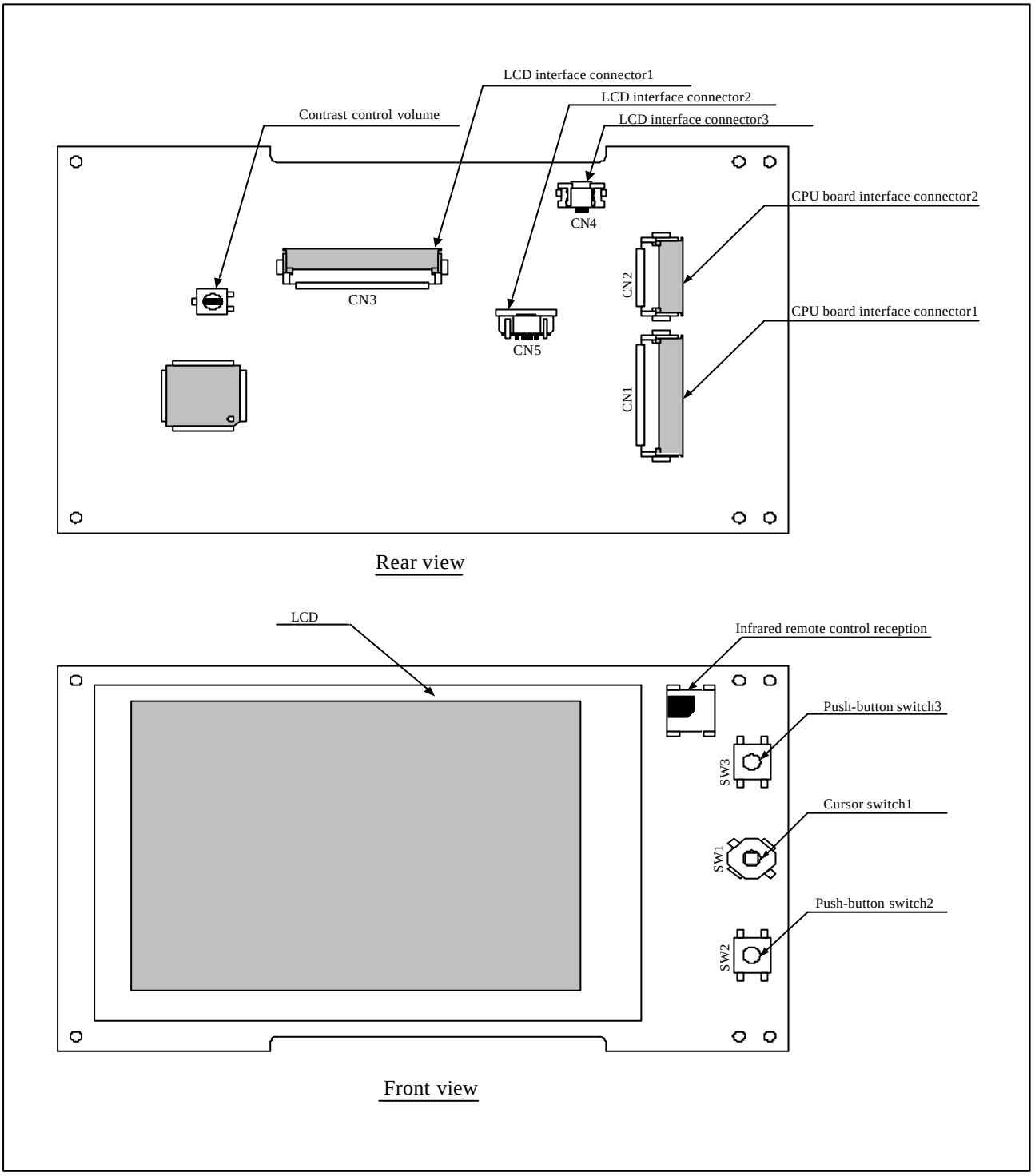
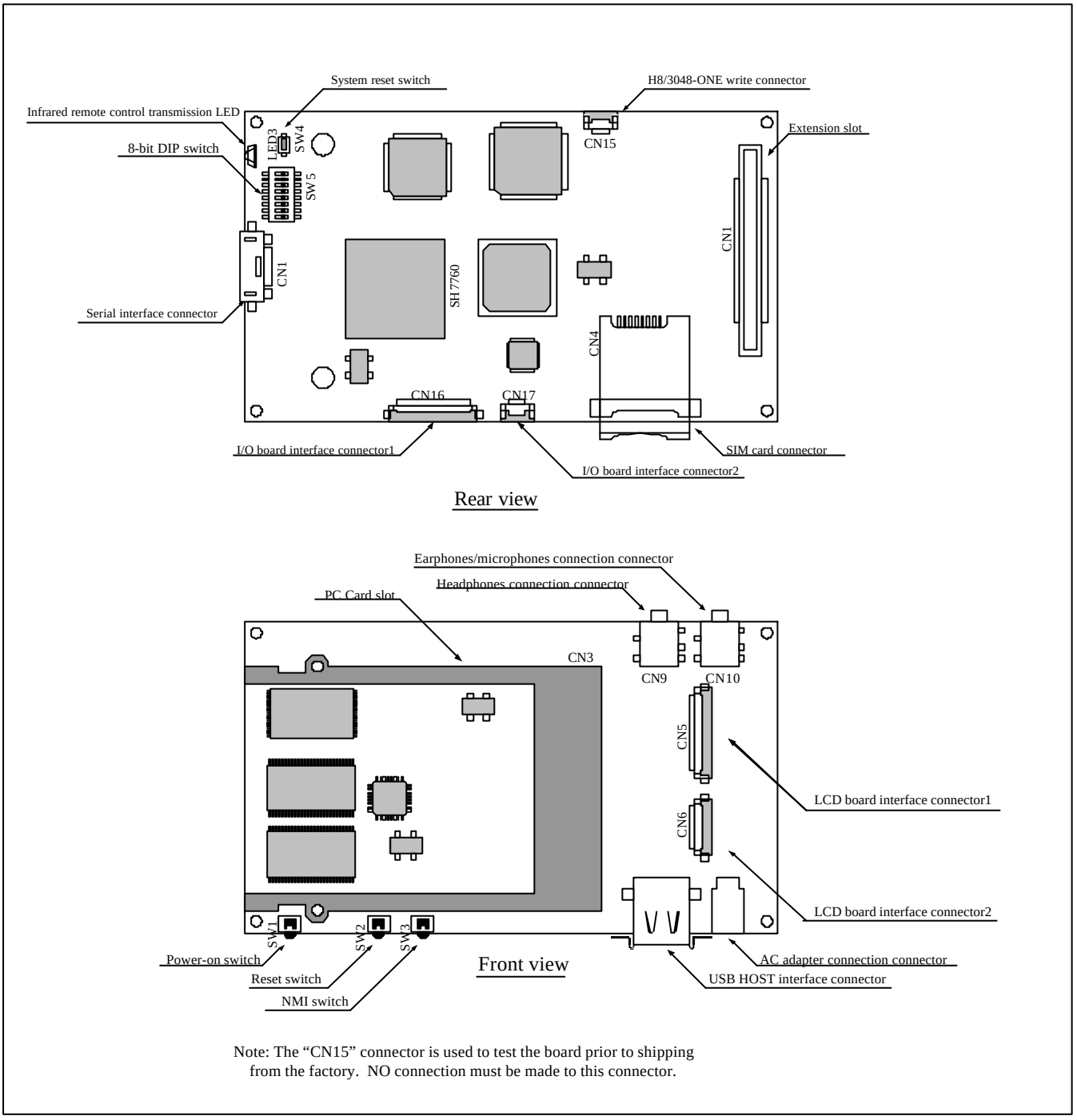


Figure 1.4 LCDBoard-External View



Note: The “CN15” connector is used to test the board prior to shipping from the factory. NO connection must be made to this connector.

Figure.1.5 CPU Board-External View

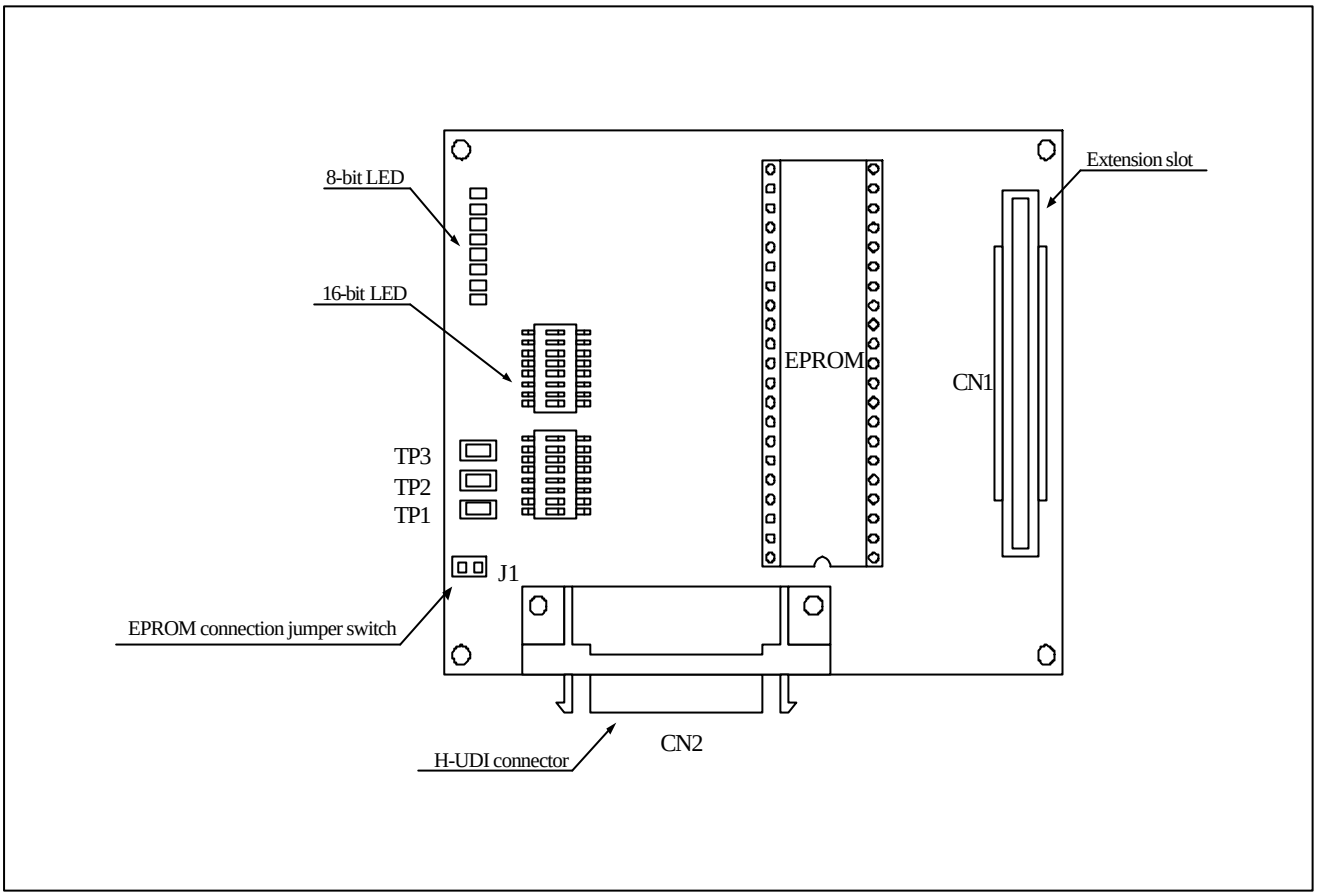


Figure 1.6 Debug Board-External View

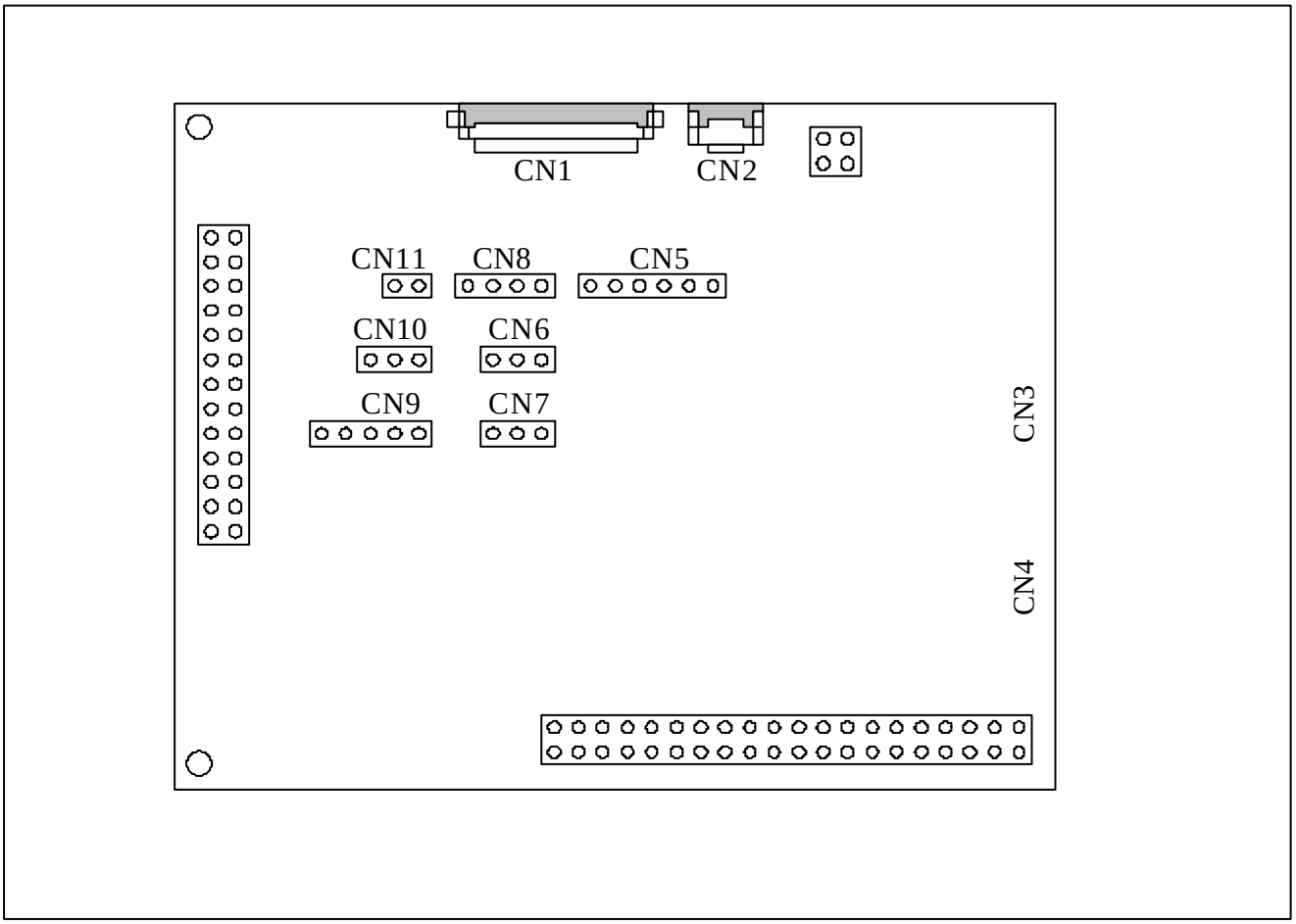


Figure 1.7 I/O Board-External View

1.4 Solution Engine2 Specifications

Table 1.1 summarizes the Solution Engine2 function specifications and Table 1.2 the power supply, dimensions and environmental specifications. In addition, Table 1.3 summarizes the permissible currents that can be supplied to the outside by Solution Engine2 supply voltages.

Table 1-1 Solution Engine2 Function Specifications

Item	Specification	Remarks
CPU	SH7760 Model name: HD6417760BP200D (Hitachi) Input clock: 16.6667MHz Operating clock (Internal): 200MHz (x 12) (External): 66MHz (x 4) Package: 256-pin BGA	
Flash Memory	Capacity: 8MB MBM29DL6409TN (Fujitsu) x 2	
SDRAM	Capacity: 64MB EDS2516APTA-75 (ELPIDA) x 2	
PC Card I/F	One slot Controller: MR-SHPC-01 V2T (Marubun) Package: 48-pin TQFP	
Serial interface	2ch Controller: ST16C2550CQ48 (EXAR) Package: 48-pin TQFP	ChA: H8/3048F-ONE interface ChB: Monitor for debugging
Sound	Model name: UDA1342TS (Phillips) Package: 28-pin SSOC Earphone/microphone: 1ch Headphone output: 1ch - Microphone input Impedance: 2.2O - Sensitivity: -51dB/Pa Headphone output Impedance: 32O	The SH7760 internal SSI is used to transfer data. The SH7760 internal SSI used to set a mode.
USB Host	1ch Controller: SH7760 internal USB host	
TFT color LCD module	Model name: NL2432DR22-02V (NEC) Display color: 262, 144 colors Display area: 240 (H) x 320 (V) Controller: SH7760 internal LCDC	
Power supply controller	H8/3084F-ONE Model name: HD64F3048BVTE25 (Hitachi) Operating frequency: 7.3728Mhz Package: 100-pin TQFP	Power supply control/RTC/Tablet interface The infrared remote control and SH7760 are interfaced via the serial chA.
RTC	Model name: ADS7843 (TI) Package: 16-pin SSOP	Via the H8/3048F-ONE
Touch panel interface	Model name: ADS7843 (TI) Package: 16-pin SSOP	Via the H8/3048F-ONE (Mounted on the LCD board)
Serial EEPROM	Capacity: 512 bytes Model name: S-29391AFJA (SII)	Via the H8/3048F-ONE
Infrared remote control	Transmission Model name: GL100MNOMP (Sharp) Transmission carrier: 38kHz Reception Model name: GP1UC101 (Sharp) Reception carrier: 38kHz	Via the H8/3048F-ONE

Table 1.2 Power supply, Dimensions and Environmental Specifications of Solution Engine2

Item	Specifications
Environment	Operating condition - Temperature: 10-35°C - Humidity: 30 to 85%RH (no dew condensation) - Ambient gas (no corrosive gas)
Operating voltage	DC 5.6V
Dissipation current	600mA
Dimensions	CPU board: 120mm x 75mm LCD board: 120mm x 75mm Debug board: 101mm x 75mm I/O board: 101mm x 75mm

Table 1.3 Permissible Current Supply to the Outside by Solution Engine2 Supply Voltages

Supply voltage	Permissible current	Devices subject to permissible current supply
5V	250mA	- PCMCIA card power supply - USB bus power - Extension slot
3.3V	250mA	- PCMCIA card power supply - Extension slot

[Notes]

(1) Table 1.2 shows the maximum dissipation current of T-Engine (comprising the CPU board, LCD board, debug board and I/O board) without external devices.

(2) Table 1.3 shows the sum of permissible current in all the powered devices on Solution Engine2. Accordingly, when a current of 100mA is used for the PCMCIA card supply voltage (5V), the currents of the USB bus power or extension slot is 150mA (250mA to 100mA). This is true for the supply voltage 3.3V.

(3) When the PCMCIS card, etc. is powered from the internal power supply of Solution Engine2, the current must not exceed the permissible current of each power supply shown in Table 1.3. Otherwise, there is a risk of electric shock, heat, or fire.

2. Installation

2.1 Host System Connection

To use the monitor program, connect the host interface connector (CN1) of Solution Engine2 to the host system with an RS-232C cross cable (accessory). Figure 2.1 shows a host system connection method. Figure 2.2 shows the pins of a serial interface connector. Table 2.1 shows the signals of the serial interface connector.

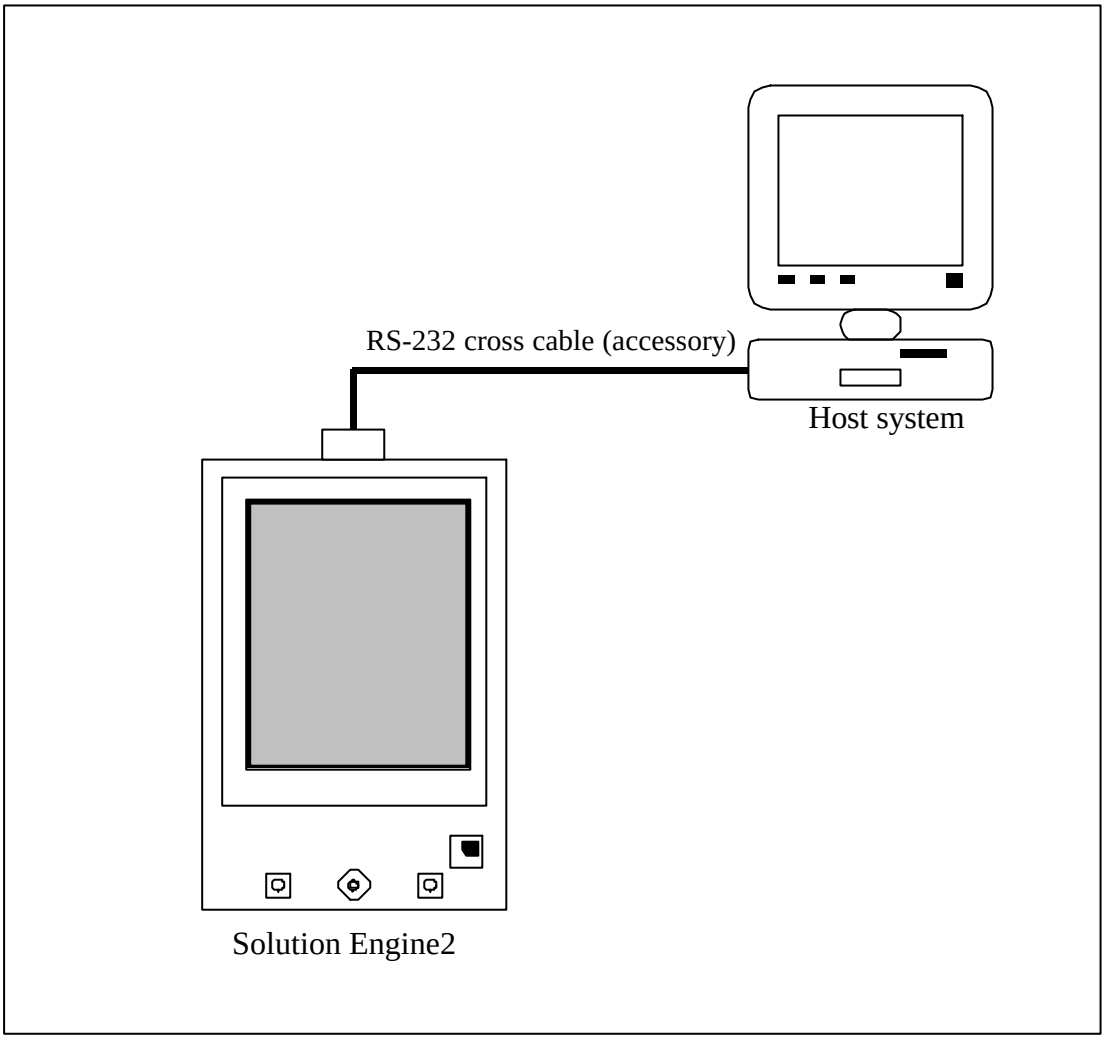


Figure 2.1 Host System Connection Method

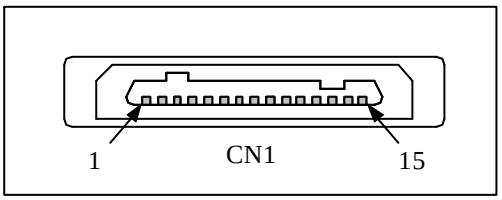


Figure 2.2 Serial Interface Connector Pin Layout

Table 2.1 Serial Interface Connector Signal Pins

Pin No	Signal name	I/O	Remarks
1	GND	-	
2	TxD	Output	TXB(UART)
3	RxD	I	RXB(UART)
4	GND	-	
5	RTS	O	RTSB(UART)
6	CTS	I	CTSB(UART)
7	GND	-	
8	Reserved	-	ISP TCK(*)
9	Reserved	-	GND(*)
10	Reserved	-	ISP TMS(*)
11	Reserved	-	ISP Plug(*)
12	Reserved	-	ISP BScan(*)
13	Reserved	-	ISP TDI(*)
14	Reserved	-	ISP TDO(*)
15	Reserved	-	Vcc(3.3V) (*)

* These pins are only used to test the board when it is shipped from the factory. Don't use these pins for other purposes.

2.2 AC Adaptor Connection

Figure 2.3 shows an AC adaptor connection method. As shown in Figure 2-3, connect the plug to the AC adaptor connector of Solution Engine2 (1), then connect the adaptor cord to the receptacle (2).

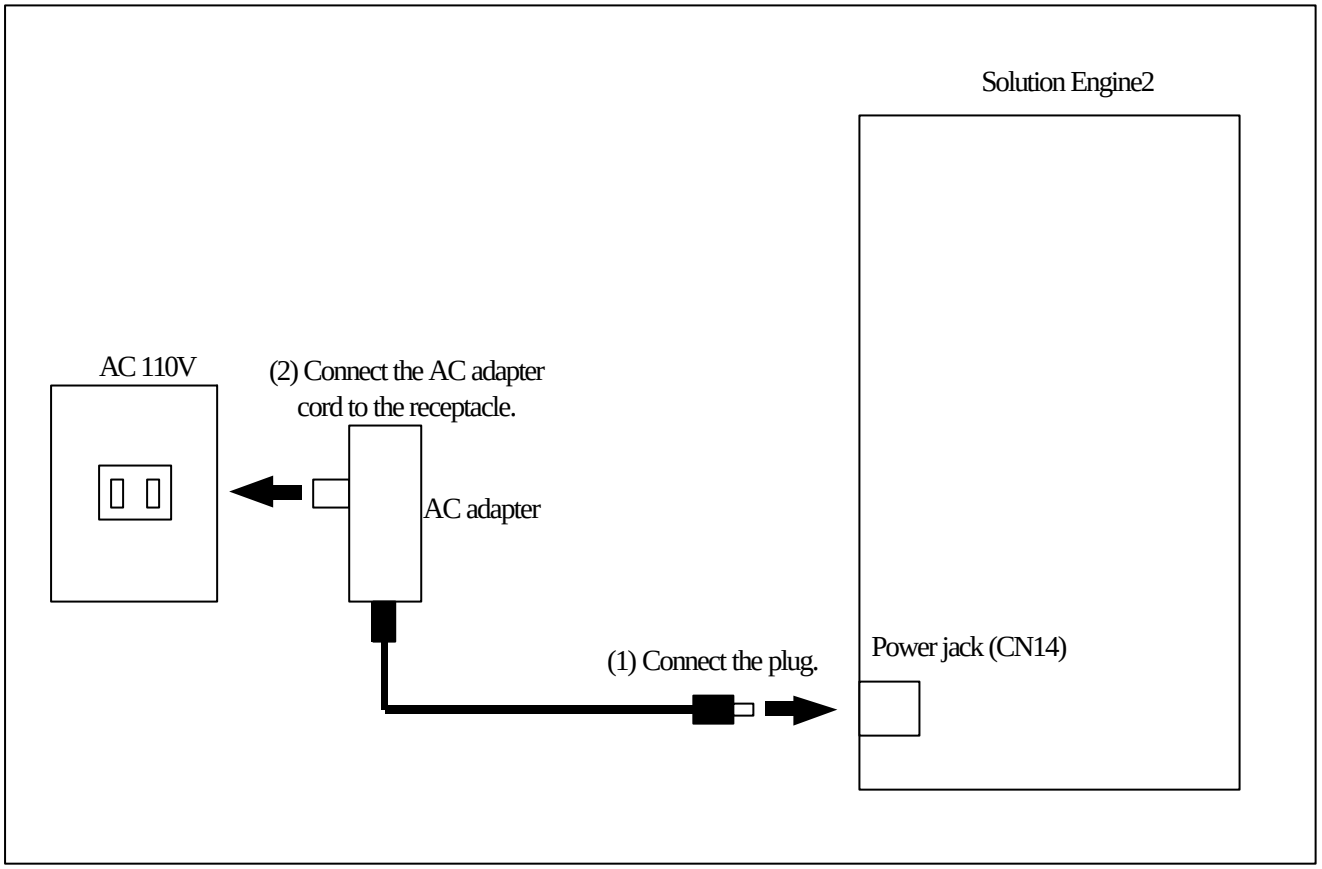


Figure 2.3 AC Adapter Connection

[Notes]

(1) Don't put a heavy item on the AC adapter cord. To avoid a risk of electric leakage, fire or electric shock, don't allow the AC adapter cord to be damaged or modified .

(2) Don't unplug the AC adapter cord with wet hand to avoid a risk of electric shock. When unplugging the cord, grasp and pull the plug instead of the cord. Don't pull the AC adapter cord to avoid a risk of cord damage, electric shock or fire.

(3) When connecting the AC adapter to the receptacle, check the polarity and connection beforehand to avoid a risk of electric shock, fire or fault.

2.3 Turning On or Off Solution Engine2

To turn on or off Solution Engine2, press the Power Switch (SW2) on the CPU board. To turn it on, press and hold down this switch for 0.5 seconds or more. To turn it off, press and hold down this switch for 4 seconds or more until Solution Engine2 is powered off.

2.4 Debug Board Usage

2.4.1 Debug Board Function

If the debug board has been connected to Solution Engine2, the following functions can be implemented.

(1) Run the program stored in the EPROM on the debug board to refresh the flash memory on the Solution Engine2 or the H8/3048-ONE firmware. For details of refreshing, refer to 10. "Flash Memory Refresh."

(2) All 8-bit LEDs on the debug board can be turned on or off from the SH7760 board. The software execution state can be monitored by controlling the ON/OFF state of these LEDs.

(3) The settings of the 16-bit switches on the SH7760 debug board can be read. These 16-bit switches can be used to control various kinds of operation conditions.

(4) The H-UDI debugger (to be connected to the H-UDI and AUD pins of the SH7760) can be used.

2.4.2 Debug Board Connection

Figure 2.4 shows a debug board connection method. Connect the debug board to the extension slot (CN4) on the Solution Engine2 board.

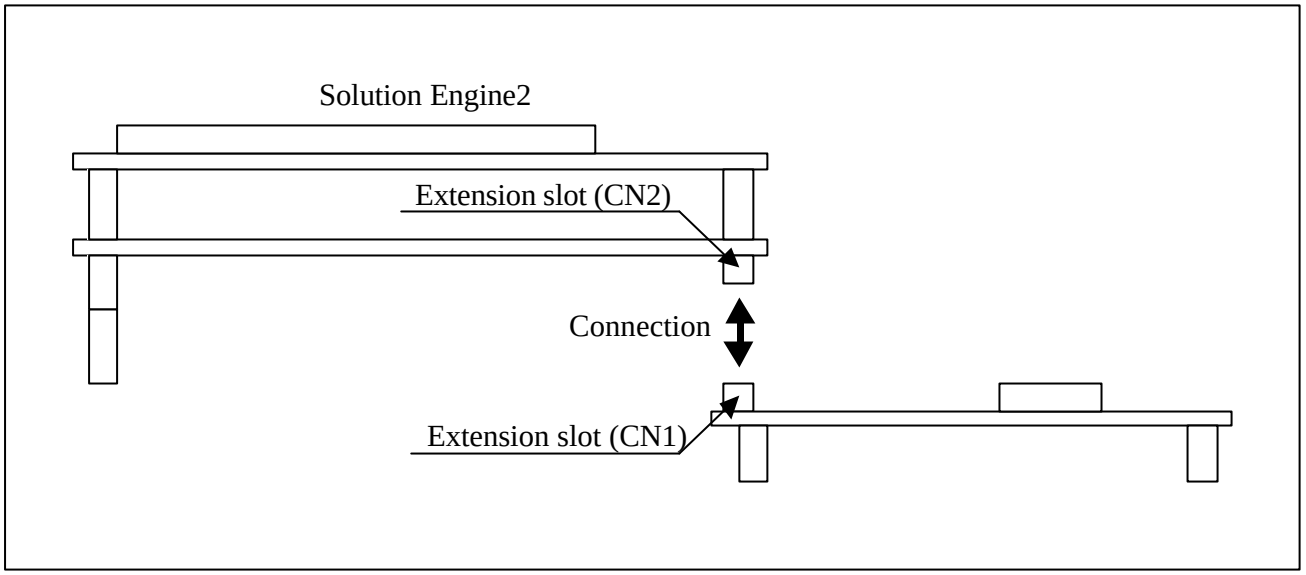


Figure 2.4 Debug Board Connection

[Notes]

When connecting the debug board or detaching the EPROM, turn off Solution Engine2 in advance. When attaching the EPROM again, check the connecting direction.

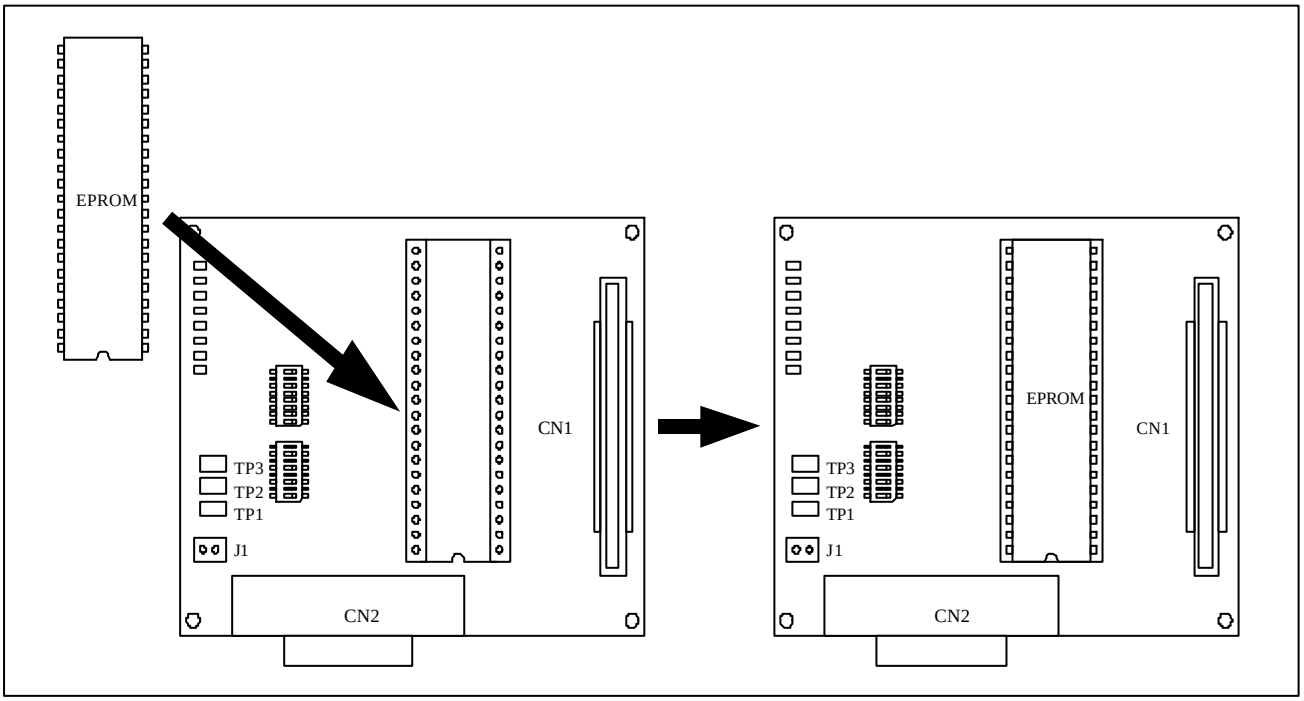
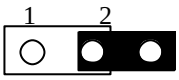


Figure 2.5 EPROM Connection

2.4.3 Debug Board Jumper Switches

Table 2.2 describes a method for setting the EPROM selection jumper switch (J1) on the debugger board. For details of a memory map during debug board connection, refer to 4. “Memory Map.”

Table 2.2 Setting the EPROM Selection Jumper Switch (J1)

Jumper switch	Setting	Description
J1	 Pins 1 and 2 are short-circuited.	Debug board resources are assigned to area 0 on the SH7760 board as shown below. (Factory setting) - The EPROM mounted on the debug board is assigned to an address range from h’00000000 to h’001FFFFF. - The 8-bit LEDs mounted on the debug board are assigned to an address range from h’00400000 to h’007FFFFF. - The 16-bit LEDs mounted on the debug board are assigned to an address range from h’00800000 to h’00BFFFFF. - The flash memory of Solution Engine2 is assigned to an address range from h’01000000 to h’017FFFFF.
	 Pins 1 and 2: OPEN	Debug board resources are assigned to area 0 on the SH7760 board as shown below. - The flash memory of Solution Engine2 is assigned to an address range from h’00000000 to h’007FFFFF. - The EPROMs mounted on the debug board are assigned to an address range from h’01000000 to h’011FFFFF - The 8-bit LEDs mounted on the debug board are assigned to an address range from h’01400000 to h’017FFFFF. - The 16-bit LEDs mounted on the debug board are assigned to an address range from h’01800000 to h’01BFFFFF.

2.4.4 8-bit LEDs on the Debug Board

The low-order 8 bits (D7 to D0) of the SH7760 data bus are connected to the 8-bit LEDs placed on the debug board. The 8-bit LEDs can be turned on or off by writing data to an area assigned for the LEDs through D7 to D0. When a value of 1 is written to a bit, the corresponding LED is turned off. When a value of 0 is written to the bit, it is turned on.

2.4.5 16-bit Switch on the Debug Board

The 16 bits (D15 to D0) of the SH7760 data bus are connected to the 16-bit switches placed on the debug board. The ON/OFF state of the 16-bit switches can be known by reading data from an area assigned for each of the switches through D15 to D0. When a value of 1 is read from a bit, the corresponding switch is set to OFF. When a value of 0 is read from the bit, it is set to ON.

2.4.6 H-UDI Debugger Connection

The debug board allows the H-UDI debugger to be connected to the pin 36 (CN2) of the H-UDI (Hitachi-User Debug Interface) connector. Connect the H-UDI and AUD pins of the SH7760 board to the H-UDI connector. Figure 2.4 shows a method for connecting the H-UDI debugger. Connect an H-UDI debugger cable to the H-UDI connector (CN2) of the debug board. Note that the following H-UDI debugger can be connected to Solution Engine2. For details on the H-UDI debugger connection/setup procedure, refer to the pertinent manual of the product.

- RENESAS Technology Corporation
  E10A Emulator Model name: HS7600KCM02H (PCMCIA)
  Model name: HS7760KCI02H (PCI)
- Hitachi ULSI Systems Co., Ltd.
  MY-ICE EZ emulator

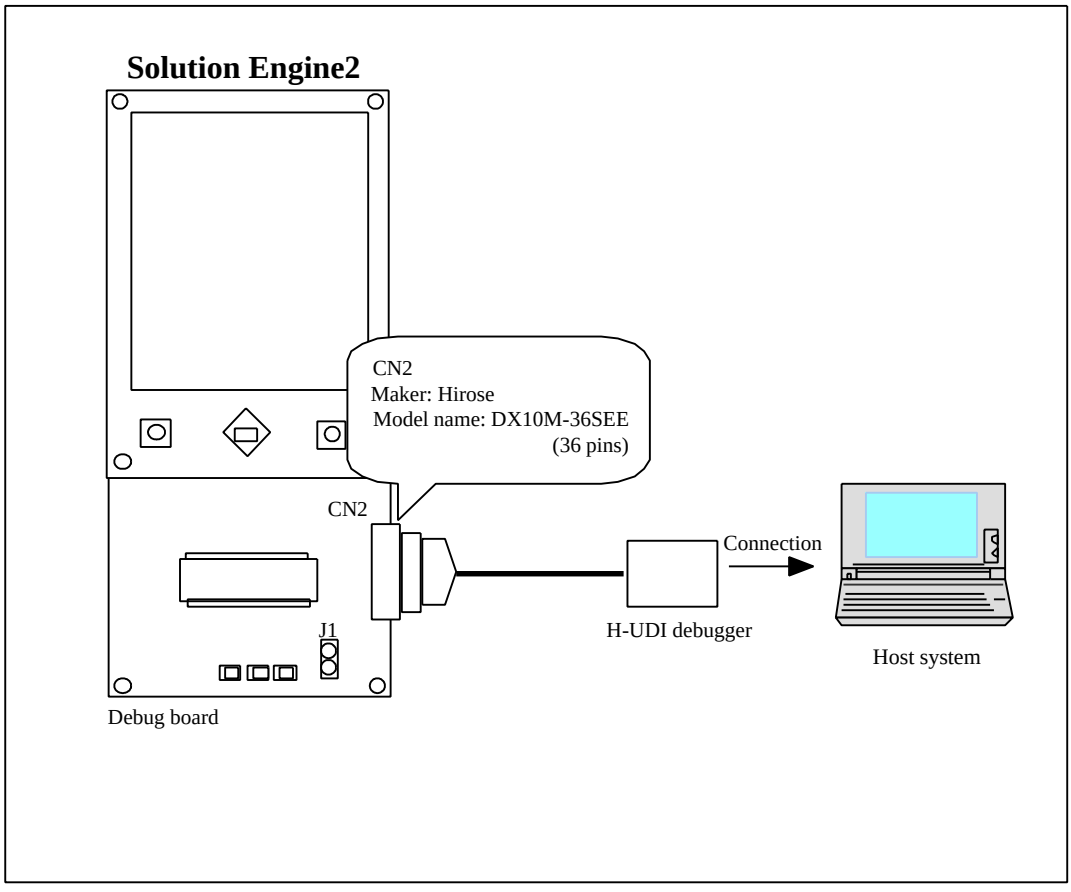


Figure 2.6 H-UDI Debugger COnnection

[Notes]

(1) Solution Engine2 permits the connection of only the H-UDI debugger that uses the AUD and H-UDI pins of the SH7760 board.

3. Switches

3.1 CPU Board Switches

Figure 3.1 shows the locations of switches (SW1 to SW5) on the CPU board. In addition, this section gives a brief description of each switch in (1) to (5).

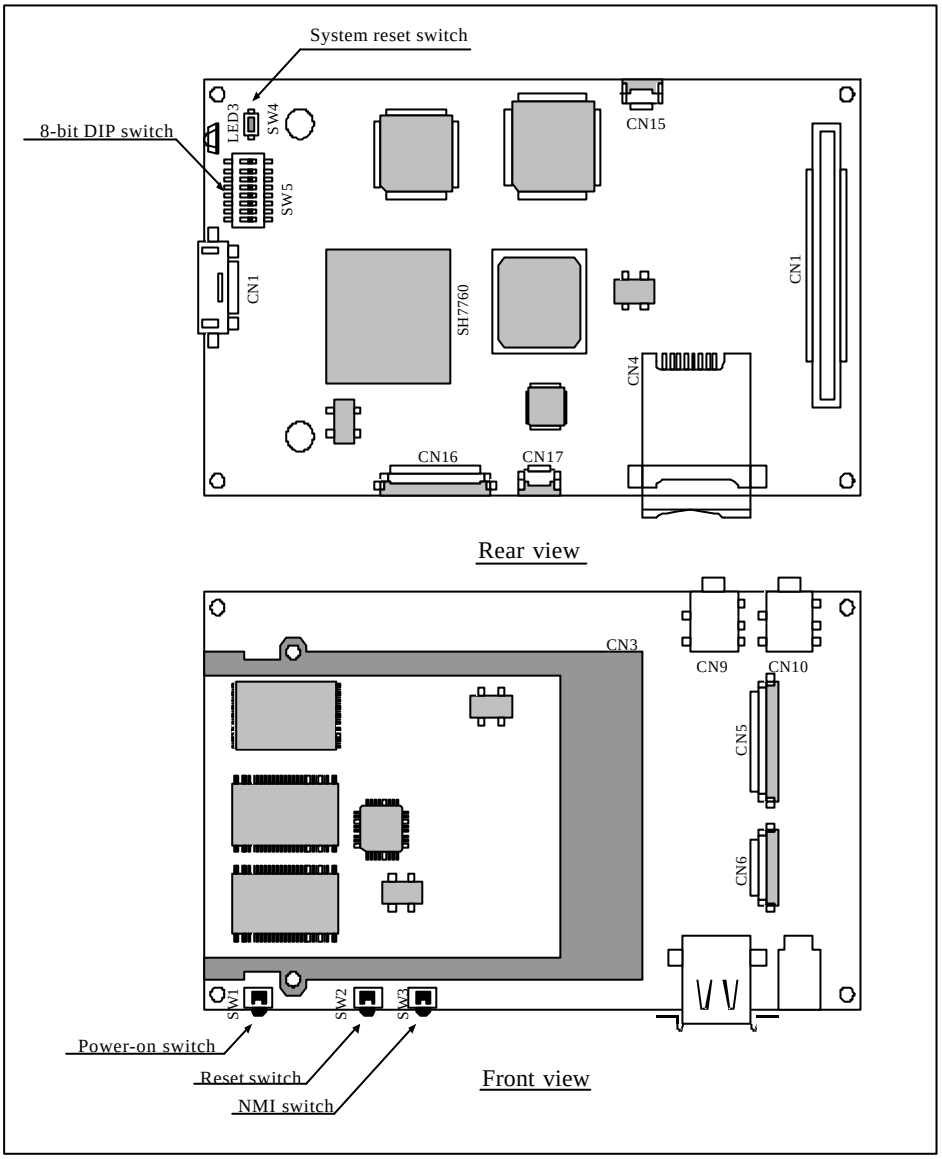


Figure 3.1 CPU Board Switches (SW1 to WS5)

(1) Power Switch (SW1)

This switch turns on or off the Solution Engine2 unit. To turn on the Solution Engine2 unit, press and hold down this switch for 0.5 seconds or more. To turn it off, press and hold down this switch for 4 seconds or more when Solution Engine2 is being powered.

(2) Reset Switch (SW2)

This switch resets Solution Engine2. To reset devices other than the H8/3048-ONE, press this switch. To reset and restart Solution Engine2, release this switch. In this case, the values of H8/3048-ONE internal registers are not initialized. Among the control registers, the values of those that can be accessed by SH7760 are initialized but the others are not (i.e., their values are retained). For more details, refer to 6.13 "Initial Values of the Power Supply Controller Register."

(3) NMI Switch (SW3)

This switch controls the SH7760 NMI pin. Press this switch and the SH7760 NMI pin will go "Low." Release this switch, and the NMI pin will go "High."

(4) 8-bit DIP Switch (SW5)

Figure 3.2 shows the setting of an 8-bit DIP switch. This DIP switch is connected to the pins ID0 to ID5 and MD5 of the ID register. Be sure to turn off the power-on switch before setting the DIP switch.

(a) Switches SW5-1 to SW5-6 are connected to pins ID0 to ID5 (input pins).

ON: The input pin goes "Low."

OFF: The input pin goes "High." (Factory setting)

(b) The SW5-7 switch is used to set the power-on condition of Solution Engine2.

ON: Solution Engine2 is powered when power supply takes place through the AC adapter.

OFF: Solution Engine2 is powered when the power-on switch is pressed. (Factory setting)

(c) The SW5-8 switch is connected to SH7760's pin MD5. The SW5-8 switch is used to set the type of endian for SH7760 operation.

ON: The MD5 pin goes "Low" to set the big endian for SH7760 operation.

OFF: The MD5 pin goes "High" to set the little endian for SH7760 operation. (Factory setting)

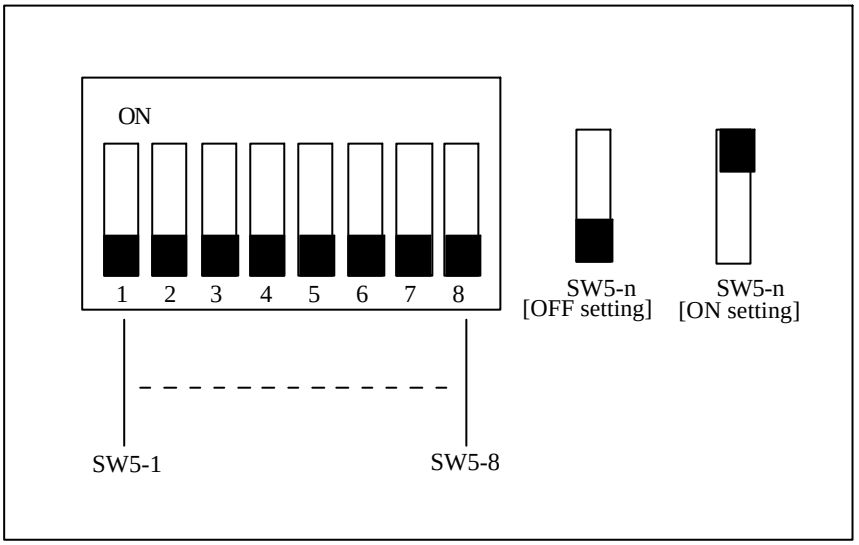


Figure 3.2 Setting the 8-bit DIP Switch

(5) System Reset Switch (SW4)

The system reset switch controls the hardware reset for Solution Engine2. All devices on Solution Emgine2 are reset while this system reset switch is pressed and held down. Solution Engine2 is turned off when this switch is released. It is turned on and activated when the power-on switch is pressed. However, Solution Emgine2 is turned on and activated if this switch is released so long as the SW5-7 switch is set ON.

3.2 LCD Board Switch

The states of the cursor switch (SW1) and push-button switches (SW2 and SW3) are signaled to the SH7760 through the power supply controller. For details, refer to 6. “Power Supply Controller.”

4. Memory Map

4.1 Memory Map for the Solution Engine2 Board

Table 4.1 shows an SH7760 memory map for the Solution Engine2 board without expansion board.

Table 4.1 SH7760 Memory Map for Solution Engine2 without Expansion Board

Area No.	Bus width	Space	Space name	Device	Remarks
CS0 area	16bit	h'00000000 ~ h'00FFFFFF	Flash memory area	8MB MBM29DL640E-90TN (Fujitsu) x 1	
		h'01000000 ~ h'03FFFFFF	-	Unused area	
CS1 area	16bit	h'04000000 ~ h' 07FFFFFF	Board control register area	16B Board control register	
CS2 area	8/16/32bit	h'08000000 ~ h'0BFFFFFF	Extension area (CS2)	64MB Extension slot (CS2 area)	Extension slot CS2# assert
CS3 area	32bit	h'0C000000 ~ h'0FFFFFFF	SDRAM area	64MB EDS2516APTA-75(ELPIDA) x 2	
CS4 area	8/16/32bit	h'10000000 ~ h'13FFFFFF	Extension area (CS4)	64MB Extension slot (CS4 area)	Extension slot CS4# assert
CS5 area	8/16/32bit	h'14000000 ~ h'17FFFFFF	Extension area (CS5)	64MB Extension slot (CS5area)	Extension slot CS5# assert
CS6 area	16bit	h'18000000 ~ h'19FFFFFF	PCMCIA area	Card controller Model name: MR-SHPC-01 V2T (Marubun) This device is simply called SH-PCIC.	
		h'1A000000 ~ h'1A7FFFFF	UART area (ChA)	UART Model name: ST16C2550CQ48 (EXAR) This device is simply called UART.	This device is used for interface with H8/3048-ONE.
		h'1A800000 ~ h'1AFFFFFF	UART area (ChB)	Same as above	This device is used for serial interface with the host.
		h'1B000000 ~ h'1BFFFFFF	ID register area		This area is used to read out the setting of a DIP switch.
CS7 area	-	h'1C000000 ~ h'1FFFFFFF	-	-	Reserved

4.2 Memory Map during Debug Board Connection

Table 4.2 shows a memory map for the SH7760 when the debug board is connected to the Solution Engine2 board and the jumper switch (J1) on the debug board is short-circuited. Table 4.2 also shows a memory map for the SH7760 when the debug board is connected to the Solution Engine2 board and the jumper switch (J1) on the debug board is open.

Table 4.2 Memory Map during Debug Board Connection (J1: Short-circuited)

Area No.	Bus width	Space	Space name	Device	Remarks
CS0 area	16bit	h'00000000 ~ h'003FFFFF	EPROM area	256kB M27C800-100F1(ST Micro) x 1	Resource on the debug board
		h'00400000 ~ h'007FFFFF	Debug LED area	1B 8-bit debug LED	
		h'00800000 ~ h'00BFFFFF	Switch area	2B 8-bit switch x 2	
		h'00C00000 ~ h'00FFFFFF	-	Unused area	
		h'01000000 ~ h'01FFFFFF	Flash memory area	8MB MBM29DL640E-90TN(Fujitsu) x 1	
		h'02000000 ~ h'03FFFFFF	-	Unused area	
CS1 area	16bit	h'04000000 ~ h'07FFFFFF	Board control register area	16B Board control register	
CS2 area	8/16/32bit	h'08000000 ~ h'0BFFFFFF	Extension area (CS2)	64MB Extension slot (CS2 area)	Extension slot CS2# assert
CS3 area	32bit	h'0C000000 ~ h'0FFFFFFF	SDRAM area	64MB EDS2516APTA-75(ELPIDA) x 2	
CS4 area	8/16/32bit	h'10000000 ~ h'13FFFFFF	Extension area (CS4)	64MB Extension slot (CS4 area)	Extension slot CS4# assert
CS5 area	8/16/32bit	h'14000000 ~ h'17FFFFFF	Extension area (CS5)	64MB Extension slot (CS5 area)	Extension slot CS5# assert
CS6 area	16bit	h'18000000 ~ h'19FFFFFF	PCMCIA area	Card controller Model name: MR-SHPC-01 V2T (Marubun) This device is simply called SH-PCIC.	
		h'1A000000 ~ h'1A7FFFFF	UART area (ChA)	UART Model name: ST16C2550CQ48 (EXAR) This device is simply called UART.	This device is used for interface with H8/3048-ONE.
		h'1A800000 ~ h'1AFFFFFF	UART area (ChB)	Same as above	This device is used for serial interface with the host.
		h'1B000000 ~ h'1BFFFFFF	ID register area		This area is used to read the setting of a DIP switch.
CS7 area	-	h'1C000000 ~ h'1FFFFFFF	-	-	Reserved

Table 4.2 Memory Map during Debug Board Connection (J1: Open)

Area No.	Bus width	Space	Space name	Device	Remarks
CS0 area	16bit	h'00000000 ~ h'00FFFFFF	Flash memory area	8MB MBM29DL640E-90TN (Fujitsu) x 1	
		h'01000000 ~ h'013FFFFF	EPROM area	256kB M27C800-100F1(ST Micro) x 1	Resource on the debug board
		h'01400000 ~ h'017FFFFF	Debug LED area	1B 8-bit debug LED	
		h'01800000 ~ h'01BFFFFF	Switch area	2B 8-bit switch x 2	
		h'01C00000 ~ h'01FFFFFF	-	Unused area	
		h'02000000 ~ h'03FFFFFF	-	Unused area	
CS1 area	16bit	h'04000000 ~ h'07FFFFFF	Board control register area	16B Board control register	
CS2 area	8/16/32bit	h'08000000 ~ h'0BFFFFFF	Extension area (CS2)	64MB Extension slot (CS2 area)	Extension slot CS2# assert
CS3 area	32bit	h'0C000000 ~ h'0FFFFFFF	SDRAM area	64MB EDS2516APTA-75 (ELPIDA) x 2	
CS4 area	8/16/32bit	h'10000000 ~ h'13FFFFF	Extension area (CS4)	64MB Extension slot (CS4 area)	Extension slot CS4# assert
CS5 area	8/16/32bit	h'14000000 ~ h'17FFFFF	Extension area (CS5)	64MB Extension slot (CS5 area)	Extension slot CS5# assert
CS6 area	16bit	h'18000000 ~ h'19FFFFFF	PCMCIA area	Card controller Model name: MR-SHPC-01 V2T (Marubun) This device is simply called SH-PCIC.	
		h'1A000000 ~ h'1A7FFFF	UART area (ChA)	UART Model name: ST16C2550CQ48 (EXAR) This device is simply called UART.	This device is used for interface with H8/3048-ONE.
		h'1A800000 ~ h'1AFFFFFF	UART area (ChB)	Same as above	This device is used for serial interface with the host.
		h'1B000000 ~ h'1BFFFFFF	ID register area		This area is used to read the setting of a DIP switch.
CS7 area	-	h'1C000000 ~ h'1FFFFFFF	-	-	Reserved

5. Functional Blocks

5.1 PCMCIA

5.1.1 Block Description

Figure 5.1 shows the PCMCIA control block. As shown in Figure 5.1, the PCMCIA control block contains a controller (MR-SHPC-01 V2 from Marubun), a 68-pin PC card interface connector (CN3) and a power supply controller IC (TPS2211DB from TI). This controller interfaces with the card(s) conforming to the PC Card Standard 97 and has the following features:

- Internal memory windows (2 windows) and I/O window (one window)
- Card access timing adjustment function
- One-step read/write buffer
- Endian internal control circuit
- Support for 5.0V/3.3V cards
- External buffer not required
- Internal interrupt steering function
- Power-down function
- Internal suspend function

There are four kinds of controller interrupts (SIRQ3 to SIRQ0). Inputs to the H7760 are made by the IRL codes. For details, refer to Marubun's MR-SHPC-01 V2 Manual.

Marubun Homepage: http://www2.marubun.co.jp

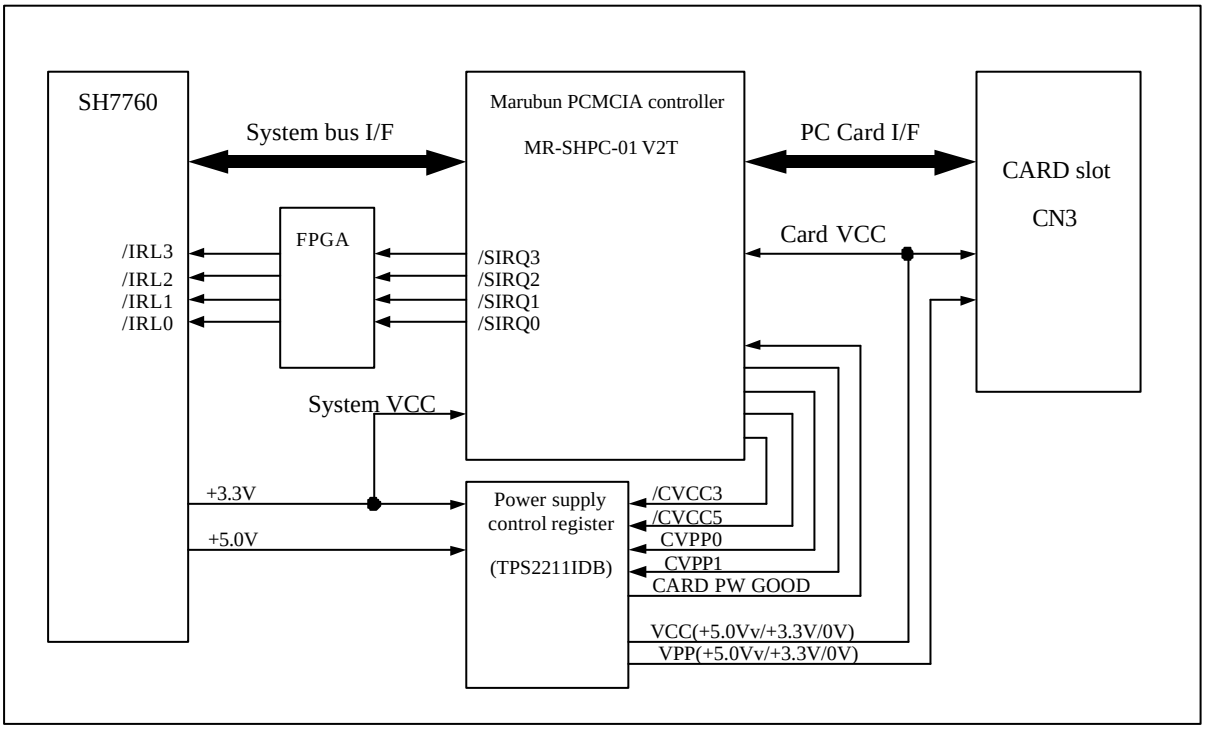


Figure 5.1 PCMCIA Controk Block

5.1.2 Connector Pins

Table 5.1 summarizes the pins of a 68-pin PC card interface connector (CN3).

Table 5.1(1) PC Card Interface Connector Signal Pins

Pin	Memory card			I/O card		
	Signal name	I/O	Function	Signal name	I/O	Function
1	GND	-	Ground	GND	-	Ground
2	D3	I/O	Data bit 3	D3	I/O	Data bit 3
3	D4	I/O	Data bit 4	D4	I/O	Data bit 4
4	D5	I/O	Data bit 5	D5	I/O	Data bit 5
5	D6	I/O	Data bit 6	D6	I/O	Data bit 6
6	D7	I/O	Data bit 7	D7	I/O	Data bit 7
7	CE1#	I	Card enable	CE1#	I	Card enable
8	A10	I	Address bit 10	A10	I	Address bit 10
9	OE#	I	Output enable	OE#	I	Output enable
10	A11	I	Address bit 11	A11	I	Address bit 11
11	A9	I	Address bit 9	A9	I	Address bit 9
12	A8	I	Address bit 8	A8	I	Address bit 8
13	A13	I	Address bit 13	A13	I	Address bit 13
14	A14	I	Address bit 14	A14	I	Address bit 14
15	WE#	I	Write enable	WE#	I	Write enable
16	READY	O	Ready	IREQ#	O	Interrupt request
17	Vcc	-	Supply voltage	Vcc	-	Supply voltage
18	VPP1	-	Programmed supply voltage	VPP1	-	Programmed supply voltage
19	A16	I	Address bit 16	A16	I	Address bit 16
20	A15	I	Address bit 15	A15	I	Address bit 15
21	A12	I	Address bit 12	A12	I	Address bit 12
22	A7	I	Address bit 7	A7	I	Address bit 7
23	A6	I	Address bit 6	A6	I	Address bit 6
24	A5	I	Address bit 5	A5	I	Address bit 5
25	A4	I	Address bit 4	A4	I	Address bit 4
26	A3	I	Address bit 3	A3	I	Address bit 3
27	A2	I	Address bit 2	A2	I	Address bit 2
28	A1	I	Address bit 1	A1	I	Address bit 1
29	A0	I	Address bit 0	A0	I	Address bit 0
30	D0	I/O	Data bit 0	D0	I/O	Data bit 0
31	D1	I/O	Data bit 1	D1	I/O	Data bit 1
32	D2	I/O	Data bit 2	D2	I/O	Data bit 2
33	WP	O	Write protect	IOIS16#	O	16-bit I/O port
34	GND	-	Ground	GND	-	Ground

Table 5.1(2) PC Card Interface Connector Signal Pins

Pin	Memory card			I/O card		
	Signal name	I/O	Function	Signal name	I/O	Function
35	GND	-	Gorund	GND	-	Gorund
36	CD1#	O	Card detection	CD1#	O	Card detection
37	D11	I/O	Data bit 11	D11	I/O	Data bit 11
38	D12	I/O	Data bit 12	D12	I/O	Data bit 12
39	D13	I/O	Data bit 13	D13	I/O	Data bit 13
40	D14	I/O	Data bit 14	D14	I/O	Data bit 14
41	D15	I/O	Data bit 15	D15	I/O	Data bit 15
42	CE2#	I	Card enable	CE2#	I	Card enable
43	VS1#	O	Voltage sense	VS1#	O	Voltage sense
44	RFU	-	Reserved	IORD#	I	I/O read
45	RFU	-	Reserved	IOWR#	I	I/O write
46	A17	I	Address bit 17	A17	I	Address bit 17
47	A18	I	Address bit 18	A18	I	Address bit 18
48	A19	I	Address bit 19	A19	I	Address bit 19
49	A20	I	Address bit 20	A20	I	Address bit 20
50	A21	I	Address bit 21	A21	I	Address bit 21
51	Vcc	-	Supply voltage	Vcc	-	Supply voltage
52	VPP2	-	Programmed supply voltage	VPP2	-	Programmed supply voltage
53	A22	I	Address bit 22	A22	I	Address bit 22
54	A23	I	Address bit 23	A23	I	Address bit 23
55	A24	I	Address bit 24	A24	I	Address bit 24
56	A25	I	Address bit 25	A25	I	Address bit 25
57	VS2#	O	Voltage sense	VS2#	O	Voltage sense
58	RESET	I	Card reset	RESET	I	Card reset
59	WAIT#	O	Bus cycle extension	WAIT#	O	Bus cycle extension
60	RFU	-	Reserved	INPACK#	O	Input port response
61	REG#	I	Register selection	REG#	I	Register selection
62	BVD2	O	Battery voltage detection	SPKR#	O	Audio digital waveform
63	BVD1	O	Battery voltage detection	STSCHG#	O	Card status change
64	D8	I/O	Data bit 8	D8	I/O	Data bit 8
65	D9	I/O	Data bit 9	D9	I/O	Data bit 9
66	D10	I/O	Data bit 10	D10	I/O	Data bit 10
67	CD2#	O	Card detection	CD2#	O	Card detection
68	GND	-	Ground	GND	-	Ground

5.1.3 Register Map

Table 5.2 shows a map for the PCMCIP controller registers. Each of the controller registers must be accessed in words.

Table 5.2 PCMCIA Control Registers

Address	Initial value	Register name
H'B83FFFE4	H'0000	Mode register
H'B83FFFE6	H'000C	Option register
H'B83FFFE8	H'03BF	Card status register
H'B83FFFEA	H'0000	Interrupt factor register
H'B83FFFEC	H'0000	Interrupt control register
H'B83FFFEE	H'0000	Card voltage control register 1
H'B83FFFF0	H'07FC	Memory window 0 Control register 1
H'B83FFFF2	H'07FC	Memory window 1 Control register 1
H'B83FFFF4	H'07FC	I/O window Control register 1
H'B83FFFF6	H'0000	Memory window 0 Control register 2
H'B83FFFF8	H'0000	Memory window 1 Control register 2
H'B83FFFFA	H'0000	I/O window Control register 2
H'B83FFFFC	H'0000	Card control register
H'B83FFFFE	H'5333	Chip information register

5.2 USB Host

5.2.1 Block Description

Figure 5.2 shows the USB host control block. As shown in Figure 5.2, the SH7760 contains an internal USB host controller. This internal controller supports USB Version 1.1 and OpenHCI, and has the following features:

- Compatibility with the OpenHCI Version 1.0 register set.
- Conforming to the USB Version 1.1
- Providing a route hub function
- Supporting the low speed (1.5Mbps) and full speed (12MB) modes
- Supporting the overcurrent detection function
- Supporting up to 127 end points
- Enabling the entire SDRAM area of area 3 (connected to the CPU) to be used for transfer data and descriptors

For more details, refer to the pertinent SH7760 Hardware Manual.

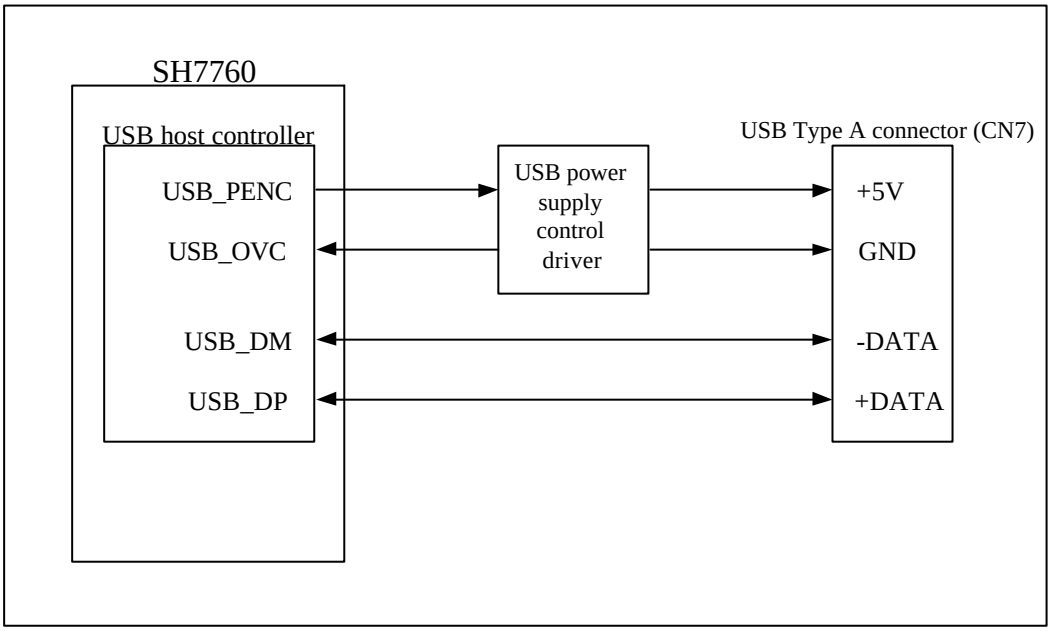
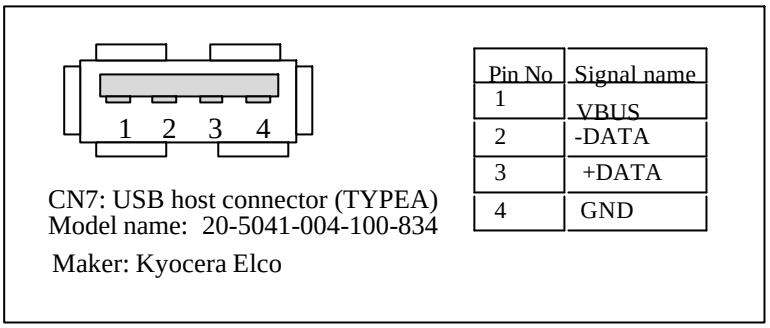


Figure 5.2 USB Host Control Block

5.2.2 Connector Pins

Figure 5.3 shows the pins of the USB host connector (CN7).



Pin No	Signal name
1	VBUS
2	-DATA
3	+DATA
4	GND

Figure 5.3 USB Host Connector (CN7) Pins

5.2.3 Register Map

Table 5.2 shows a register map for the SH7727 internal USB host controller registers.

Table 5.3 USB Host Controller Register

Address	Initial value	Register name
H'FE340000	H'00000010	HcRevision register
H'FE340004	H'00000000	HcControl register
H'FE340008	H'00000000	HcCommandStatus register
H'FE34000C	H'00000000	HcInterruptStatus register
H'FE340010	H'00000000	HcInterruptEnable register
H'FE340014	H'00000000	HcInterruptDisable register
H'FE340018	H'00000000	HcHCCA register
H'FE34001C	H'00000000	HcPeriodCurrentED register
H'FE340020	H'00000000	HcControlHeadED register
H'FE340024	H'00000000	HcControlCurrentED register
H'FE340028	H'00000000	HcBulkHeadED register
H'FE34002C	H'00000000	HcBulkCurrentED register
H'FE340030	H'00000000	HcDonrHeadED register
H'FE340034	H'00002EDF	HcFmInterval register
H'FE340038	H'00000000	HcFrameRemaining register
H'FE34003C	H'00000000	HcFmNumber register
H'FE340040	H'00000000	HcPeriodicStart register
H'FE340044	H'00000628	HcLSThreshold register
H'FE340048	H'02001202	HcRhDescriptorA register
H'FE34004C	H'00000000	HcRhDescriptorB register
H'FE340050	H'00000000	HcRhStatus register
H'FE340054	H'00000100	HcRhPortStatus1 register
H'FE341000 ~ H'FE342FFF	-	Shared memory area

5.3 UART

5.3.1 Block Description

Figure 5.4 shows the UART control block. As shown in Figure 5.4, the UART control block contains a controller (ST16C2550 from EXAR), RS232C interface driver and 15-pin connector (CN1). This controller uses the clock pulses (7.3728MHz) supplied from the power supply controller (H8/3048F-ONE) for operations, and determines a baud rate (transfer rate) using these pulses as reference.

This controller has been provided with a 2-channel UART device. Channel A is used to communicate with the power supply controller (H8/3048F-ONE). Because channel B is connected to a 15-pin RS-232C connector (CN1), it can be used as a debug interface if it is connected to a PC.

In addition, channel A (INTA) inputs the controller interrupts to the SH7760 IRL9 and channel B (INTB) inputs them to the SH7760 IRL11.

For more details, refer to EXAR's ST16C2550 Manual.

EXAR Homepage: http://www.exar.com

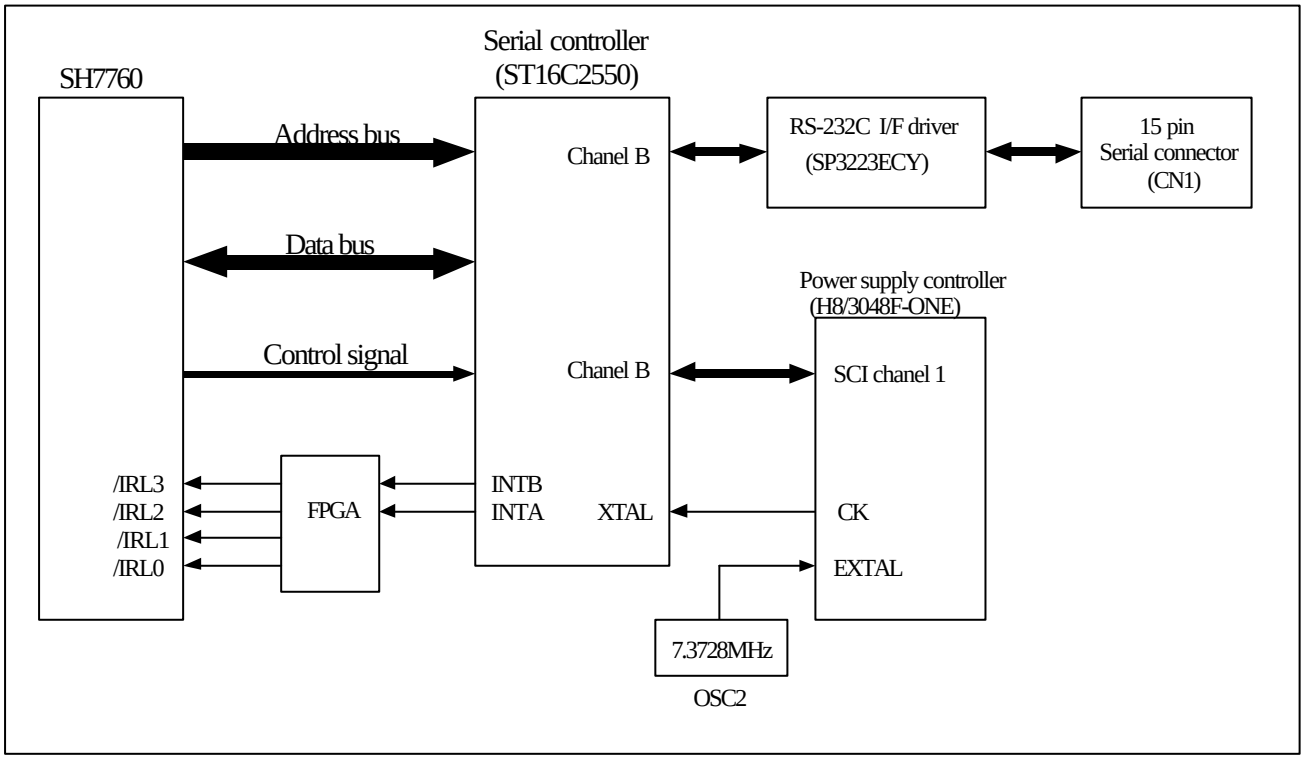
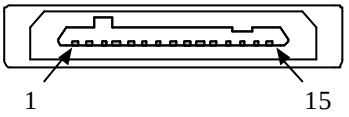


Figure 5.4 Serial Interface Block

5.3.2 Connector Pins

Figure 5.5 shows the pins of a 15-pin serial interface connector (CN1).



CN1: 15-pin serial connector

Model name: RMC-EA15MY-OM15-MC1

Moker: Honda Tsushin Kogyo

Pin No	Signal name
1	GND
2	TxD
3	RxD
4	GND
5	RTS
6	CTS
7	GND
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved

Figure 5.5 15-pin Serial Interface Connector Pins

5.3.3 Register Map

Tables 5.4 and 5.5 show register maps for the serial interface controller registers. Each of the serial interface controller registers must be accessed in words. If access takes place in words, data in the low order 8 bits (D7 to D0) will become effective.

Table 5.4 Serial Interface Control Register Map (Channel A)

Address	Initial value	Register name (at resd)	Register name (at write)	Remarks
H'BA000000	-	RHR (Receive Holding Register)	THR (Transfer Holding Register)	LCR bit7=0
H'BA000000	-	DLL (LSB of Divisor Latch)	DLL (LSB of Divisor Latch)	LCR bit7=1
H'BA000002	H'00	IER (Interrupt Enable Register)	IER (Interrupt Enable Register)	LCR bit7=0
H'BA000002	-	DLM (MSB of Divisor Latch)	DLM (MSB of Divisor Latch)	LCR bit7=1
H'BA000004	H'01	ISR (Interrupt Status Register)	FCR (FIFO Control Register)	
H'BA000006	H'00	LCR (Line Control Register)	LCR (Line Control Register)	
H'BA000008	H'00	MCR (Modem Control Register)	MCR (Modem Control Register)	
H'BA00000A	H'60	LSR (Line Status Register)	N.A	
H'BA00000C	H'X0	MSR (Modem Status Register)	N.A	
H'BA00000E	H'FF	SPR (Scratchpad Register)	SPR (Scratchpad Register)	

Table 5.5 Serial Interface Control Register Map (Channel B)

Address	Initial value	Register name (at resd)	Register name (at write)	Remarks
H'BA800000	-	RHR (Receive Holding Register)	THR (Transfer Holding Register)	LCR bit7=0
H'BA800000	-	DLL (LSB of Divisor Latch)	DLL (LSB of Divisor Latch)	LCR bit7=1
H'BA800002	H'00	IER (Interrupt Enable Register)	IER (Interrupt Enable Register)	LCR bit7=0
H'BA800002	-	DLM (MSB of Divisor Latch)	DLM (MSB of Divisor Latch)	LCR bit7=1
H'BA800004	H'01	ISR (Interrupt Status Register)	FCR (FIFO Control Register)	
H'BA800006	H'00	LCR (Line Control Register)	LCR (Line Control Register)	
H'BA800008	H'00	MCR (Modem Control Register)	MCR (Modem Control Register)	
H'BA80000A	H'60	LSR (Line Status Register)	N.A	
H'BA80000C	H'X0	MSR (Modem Status Register)	N.A	
H'BA80000E	H'FF	SPR (Scratchpad Register)	SPR (Scratchpad Register)	

5.4 LCD

5.4.1 Block Description

Figure 5.6 shows the LCD control block. As shown in Figure 5.6, the LCD control block contains an SH7760 internal LCD controller and an LCD panel (TFT liquid crystal panel) mounted on the LCD board that can display 16-bit RGB data with a resolution of QVGA (240 x 320). In addition, the SRAM allocated to area 3 is used for the LCD display VRAM (Video RAM).

Display data is stored in the order of coordinates (0,0), (1,0), … (239, 319) from the address set in the LCD controller register (LDSARU). On the LCD panel display, data at the upper left corner is handled as data on the origin (0,0) and data at the lower right corner is handled as data on the coordinates (239,319).

The front light on the LCD panel can be turned on or off by the power supply controller. For details on front light control, refer to 6. “Power Supply Controller.” In addition, refer to the pertinent SH7760 Hardware Manual for details on the LCD controller.

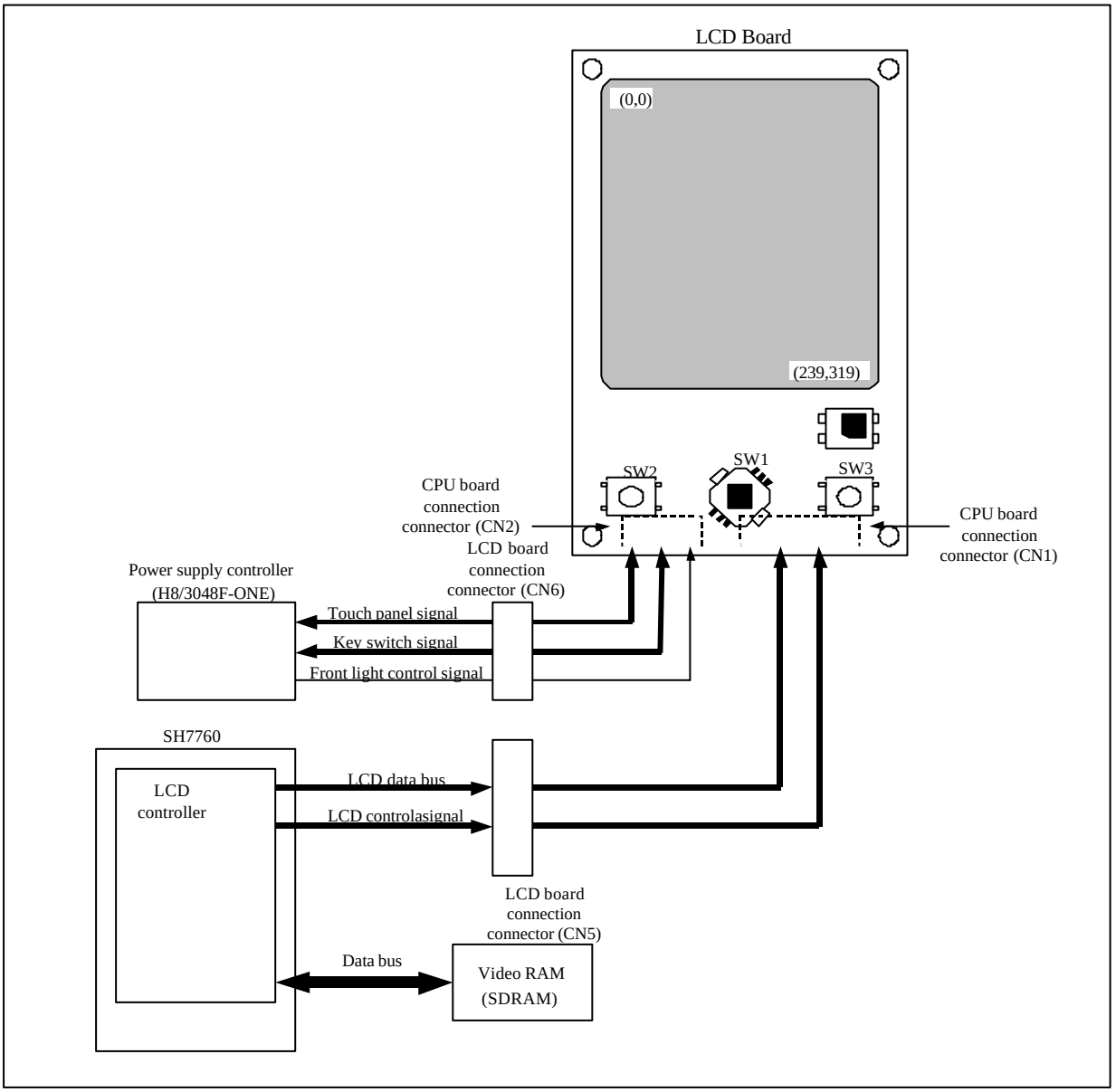


Figure 5.6 LCD Control Block

5.4.2 Connector Pins

Figure 5.7 shows the pins of the LCD interface connectors (CN5 and CN6). Tables 5.6 and 5.7 summarize the signals of these interface connectors.

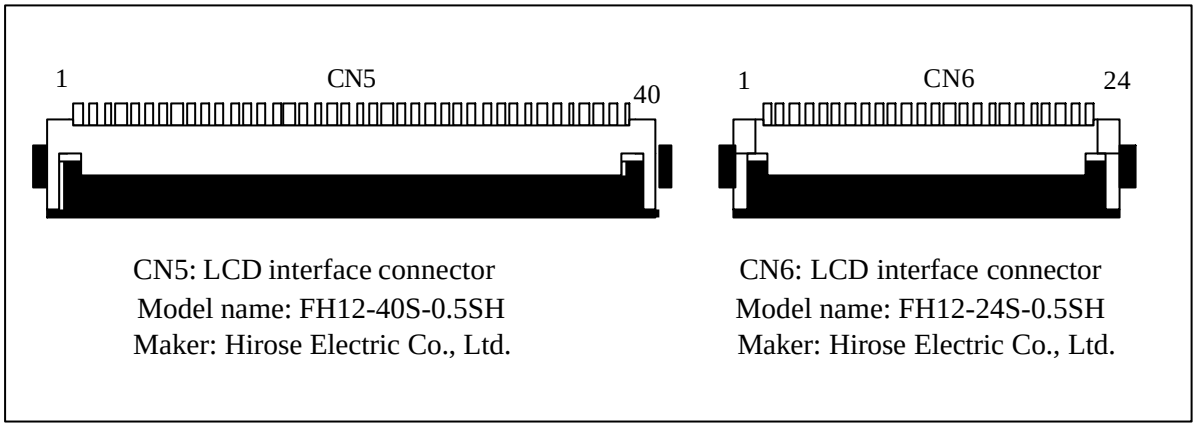


Figure 5.7 LCD Interface Connector (CN5/CN6) Pins

Table 5.6 LCD Interface Connector (CN5) Signals

Pin No.	Signal name	I/O	Remarks	Pin No.	Signal name	I/O	Remarks
1	VBAT	-	Power supply	21	LCD13	OUT	LCDC
2	VBAT	-	Power supply	22	LCD14	OUT	LCDC
3	VBAT	-	Power supply	23	LCD15	OUT	LCDC
4	VBAT	-	Power supply	24	GND	-	Power supply
5	N.C	-	Unused	25	GND	-	Power supply
6	LCD0	OUT	LCDC	26	CL1	OUT	LCDC
7	LCD1	OUT	LCDC	27	CL2	OUT	LCDC
8	LCD2	OUT	LCDC	28	DON	OUT	LCDC
9	LCD3	OUT	LCDC	29	M_DISP	OUT	LCDC
10	LCD4	OUT	LCDC	30	FLM	OUT	LCDC
11	LCD5	OUT	LCDC	31	VEPWC	OUT	LCDC
12	LCD6	OUT	LCDC	32	VCPWC	OUT	LCDC
13	LCD7	OUT	LCDC	33	NC	-	Unused
14	GND	-	Power supply	34	GND	-	Power supply
15	GND	-	Power supply	35	GND	-	Power supply
16	LCD8	OUT	LCDC	36	IR_IN	IN	Remote control
17	LCD9	OUT	LCDC	37	3.3V	-	Power supply
18	LCD10	OUT	LCDC	38	3.3V	-	Power supply
19	LCD11	OUT	LCDC	39	3.3V	-	Power supply
20	LCD12	OUT	LCDC	40	3.3V	-	Power supply

Table 5.7 LCD Interface Connector (CN6) Signals

Pin No.	Signal name	I/O	Remarks	Pin No.	Signal name	I/O	Remarks
1	GND	-	Power supply	13	~PAD_CS	OUT	PAD I/F
2	GND	-	Power supply	14	~PAD_IRQ	IN	PAD_I/F
3	KEY_IN0	IN	KEY_I/F	15	PAD_DIN	OUT	PAD_I/F
4	KEY_IN1	IN	KEY_I/F	16	PAD_DOUT	IN	PAD_I/F
5	KEY_IN2	IN	KEY_I/F	17	PAD_DCLK	OUT	PAD_I/F
6	KEY_IN3	IN	KEY_I/F	18	~RESET	OUT	Reset
7	KEY_IN4	IN	KEY_I/F	19	~LCD_FLON	OUT	LCD Power supply
8	KEY_OUT0	OUT	KEY_I/F	20	~LCD_PWRDY	IN	LCD Power supply
9	KEY_OUT1	OUT	KEY_I/F	21	GND	-	Power supply
10	KEY_OUT2	OUT	KEY_I/F	22	GND	-	Power supply
11	GND	-	Power supply	23	3.3VSB	-	Power supply
12	GND	-	Power supply	24	3.3VSB	-	Power supply

5.4.3 Register Map

Table 5.8 shows a register map for the SH7760 internal LCD controller.

Table 5.8 LCD Controller Registers

Address	Initial value	Register name
H'FE300C00	H'0101	Input clock register
H'FE300C02	H'0109	Module type register
H'FE300C04	H'000C	Data format register
H'FE300C06	H'0000	Scan mode register
H'FE300C08	H'0C000000	Data fetch start address register for data on the display top
H'FE300C0C	H'0C000000	Data fetch start address register for data on the display bottom
H'FE300C10	H'0280	Fetch data line address offset register for display data
H'FE300C12	H'0000	Palette control register
H'FE300800~ H'FE300BFC	-	Palette data register
H'FE300C14	H'4F52	Horizontal character count register
H'FE300C16	H'0050	Horizontal synchronization signal register
H'FE300C18	H'01DF	Vertical display line count register
H'FE300C1A	H'01DF	Vertical total line count register
H'FE300C1C	H'01DF	Vertical synchronization signal register
H'FE300C1E	H'000C	AC modulation signal toggle line count register
H'FE300C20	H'0000	Interrupt control register
H'FE300C24	H'0010	Power management mode register
H'FE300C26	H'F60F	Power supply control sequence duration register
H'FE300C28	H'0000	Control register

5.5 Sound Generator

5.5.1 Block Description

Figure 5.8 shows the sound generator control block. As shown in Figure 5.8, this control block contains an SH7760 internal serial sound interface (SSI) and an audio CODEC (UDA1342TS from Phillips) so that sound can be output to headphones connected to an output mini-jack (CN9) or it can be input to earphones connected to an I/O mini-jack (CN10). In addition, headphone output takes place with the quality of stereo output while earphone I/O takes place with the quality of monaural I/O that uses only the Rch.

This control block is connected to an electronic volume so that sound output volume can be controlled via the generator. The electronic volume is controlled by the power supply controller. For details, refer to 6. “Power Supply Controller.” In addition, Solution Engine2 has the following characteristics for microphone input and headphone output:

- Microphone input

  Impedance: 2.2KO

  Sensitivity: -51dB/Pa

- Headphone output

  Impedance: 32O

For more details, refer to the pertinent SH7760 Hardware Manual and Phillips UDA1342TS Manual.

Phillips Homepage: http://www.semiuconductors.phillips.com

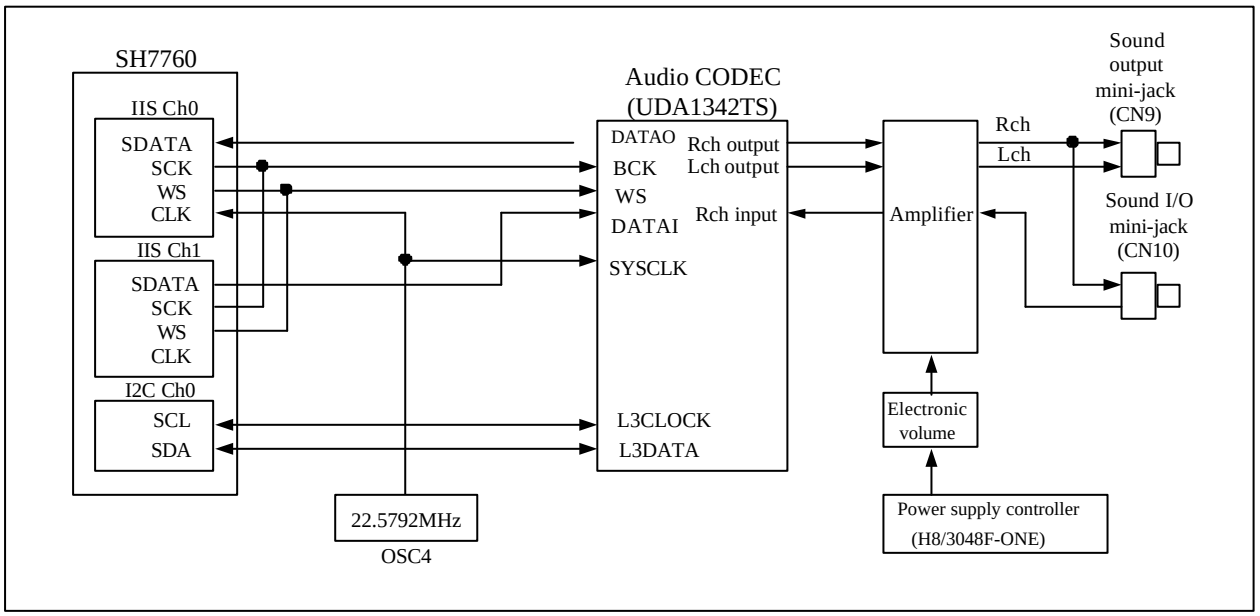


Figure 5.8 Sound Generator Control Block

5.5.2 Connector Pins

Figure 5.9 shows the pins of the sound generator I/O mini-jack (CN9, CN10). Tables 5.9 and 5.10 list the signals of the sound generator I/O mini-jack (CN9, CN10).

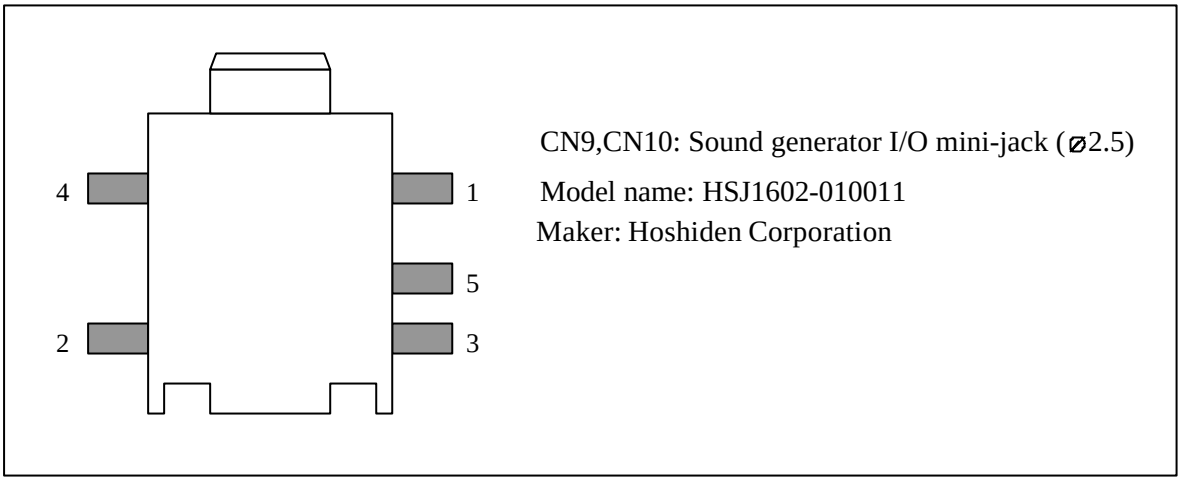


Figure 5.9 Sound Generator I/O Mini-jack (CN9, CN10)

Table 5.9 Sound Generator I/O Mini-jack (CN9) Signals

Pin No	Signal name
1	GND
2	R-IN
3	R-OUT
4	MIC-IN
5	HP_SENSE

Table 5.10 Sound Generator I/O Mini-jack (CN10) Signals

Pin No	Signal name
1	GND
2	L-OUT
3	R-OUT
4	HP_SENSE
5	NC

5.5.3 Register Map

Table 5.11 shows a register map for the SH7760 internal serial sound interface (SSI).

Table 5.11 SSI Control Registers

Register abbreviation	Address	R/W	Initial value	Access size
SSICR0	H'FE680000	R/W	H'0000 0000	32
SSISR0	H'FE680004	R/W	H'0200 0003	32
SSITDR0	H'FE680008	R	H'0000 0000	32
SSIRDR0	H'FE68000C	R	H'0000 0000	32
SSICR1	H'FE690000	R/W	H'0000 0000	32
SSISR1	H'FE690004	R/W	H'0200 0003	32
SSITDR1	H'FE690008	R	H'0000 0000	32
SSIRDR1	H'FE69000C	R	H'0000 0000	32

5.6 SIM Card Interface

5.6.1 Block Description

Figure 5.11 shows the SIM card interface control block. As shown in Figure 5.11, this control block contains an SH7760 internal SIM card module (SIM), a power supply/level converter (LTC1555LEGN-1, 8) and an 8-pin connector (CN4) to enable communications with the SIM card inserted into the SIM card interface connector (CN4).

SIM card reset can be controlled through SIM SIM_RST control. The following methods can be used for reset control.

- "Low" output from SIM_RST: The SIM card reset pin is set to "Low." (Reset)
- "High" output from SIM_RST: The SIM card reset pin is set to "High." (Normal)

Power supply to the SIM card is controlled through the power supply controller (H8/3048f-ONE). The SIM card is being powered while Solution Engine2's power is turned on. Before inserting or removing the SIM card, be sure to turn off the Solution Engine2 unit.

For more details, refer to the pertinent SH7760 Hardware Manual.

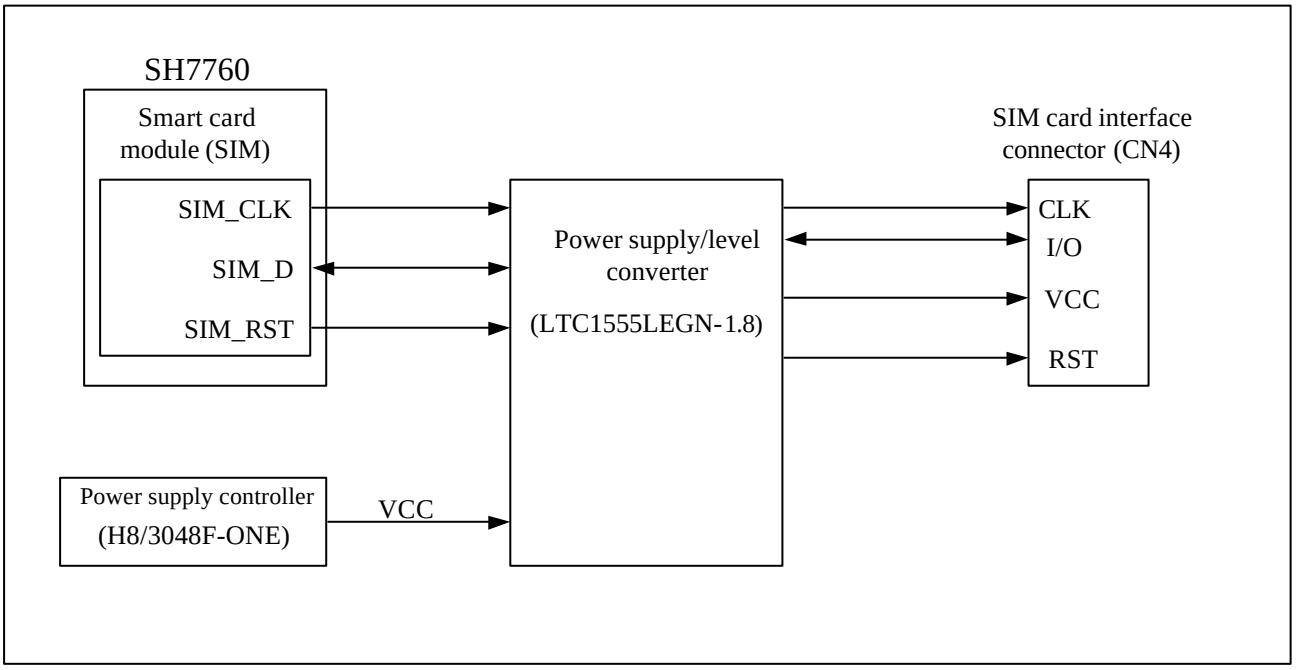


Figure 5.11 eTROM Interface Control Block

5.6.2 Connector Pins

Figure 5.12 shows the pins of the SIM card interface connector (CN4) and Table 5.12 lists the signals of that connector.

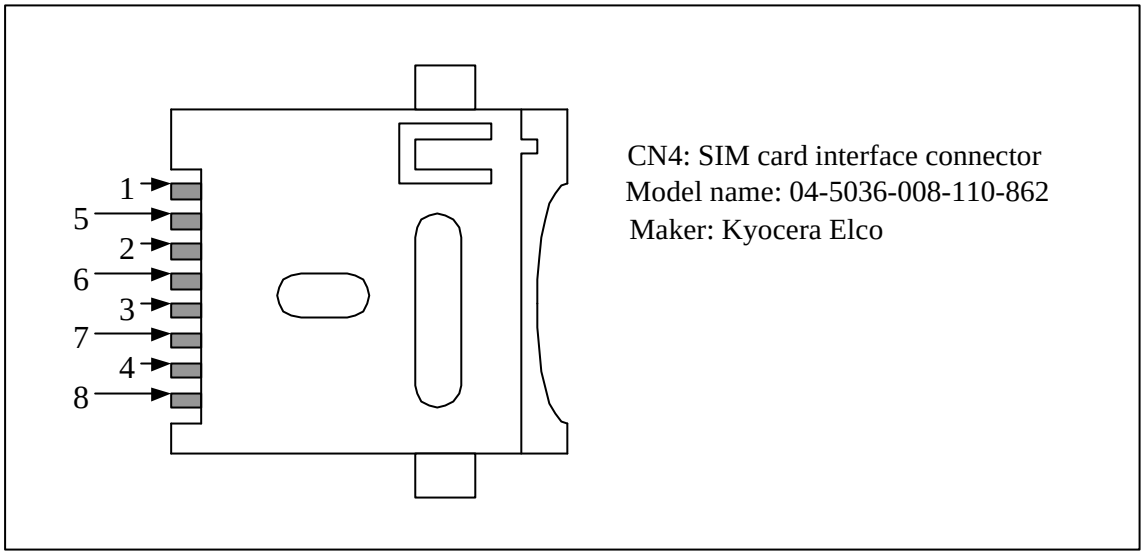


Figure5.12 SIM Card Interface Connector (CN4) Pins

Table 5.12 SIM Card Interface Connector (CN4) Signals

Pin No	Signal name
1	C1:VCC
2	C2:RST
3	C3:CLK
4	C4:*1
5	C5:GND
6	C6:VPP
7	C7:I/O
8	C8: *1

*1 Don’t use the pins 4 and 8 because they must be connected to the board test connector (CN13).

5.6.3 Register Map

Table 5.13 shows a register map for the SH7760 internal SIM card module (SIM).

Table 5.13 SIM Card Module Register Map

Address	Initial value	Register name
H'FE480000	H'20	Serial mode register
H'FE480002	H'07	Bit rate register
H'FE480004	H'00	Serial control register
H'FE480006	H'FF	Transmit data register
H'FE480008	H'84	Serial status register
H'FE48000A	H'00	Received data register
H'FE48000C	H'01	Smart card mode register
H'FE48000E	H'00	Serial control 2 register
H'FE480010	H'0000	Wait time register
H'FE480012	H'00	Guard extension register
H'FE480014	H'0173	Sample register

6. Power Supply Controller

6.1 Power Supply Controller Functions

The H8/3048F-ONE power supply controller (simply called the power supply controller) provides the following control functions by firmware stored in the internal memory. The following functions can be controlled through the UART ChA from the SH7760. Figure 6.1 shows a power supply control block diagram.

(1) RTC (real-time clock) function
(2) System power supply (3.3V/5/0V) ON/OFF control function
(3) Touch panel coordinate position read function
(4) Key switch input function
(5) Infrared remote control transmission/reception function
(6) Electronic volume
(7) Serial EPROM read/write function

These functions can be controlled through the UART chA from SH7760.

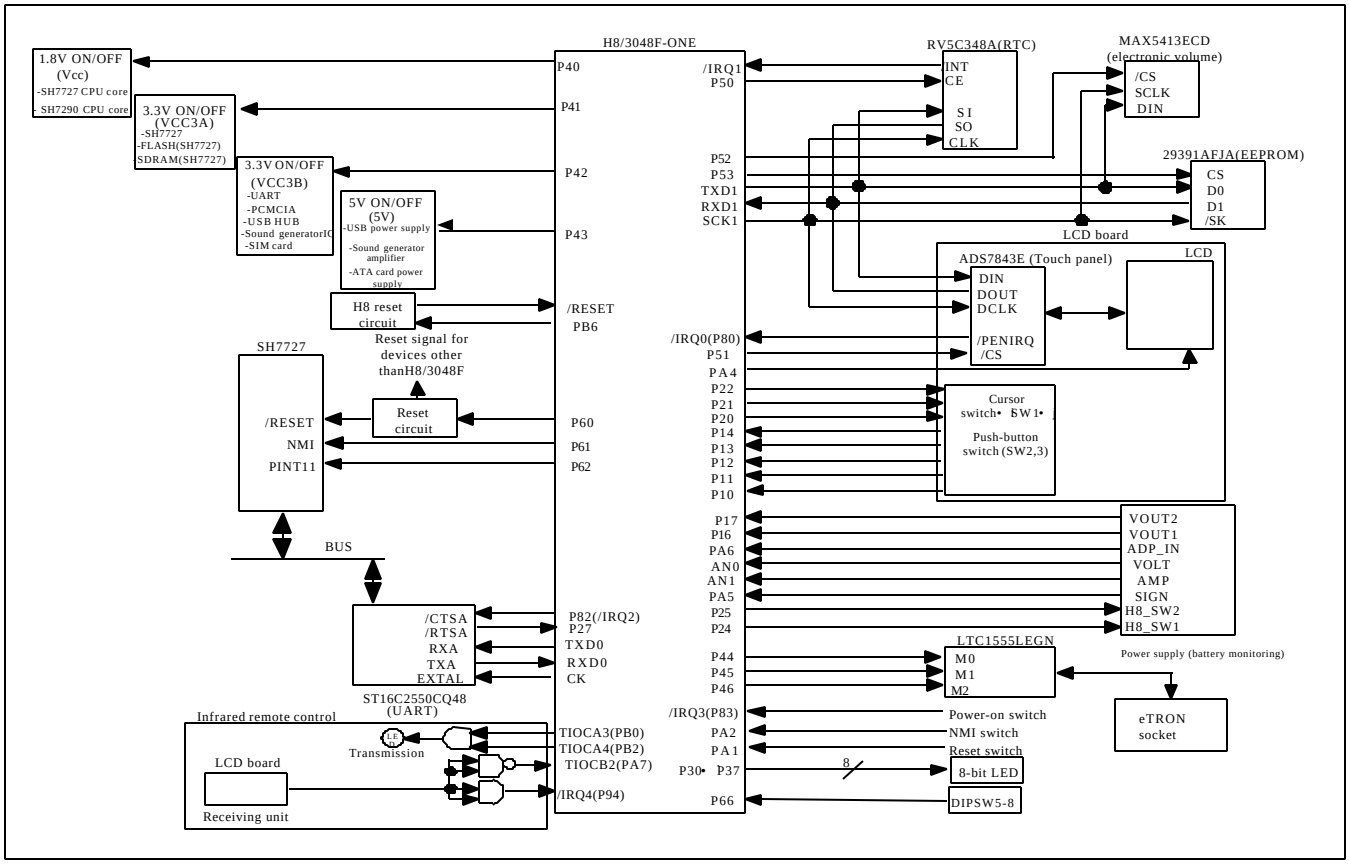


Figure 6.1 Power Supply Control Block Diagram

[Notes]

Though the power supply controller's I/O port is connected to the /RTSA and /CTSA pins of the UART controller (ST16C2550) through the circuit, the power supply controller does not execute hardware control during communications with SH7760. For details of communications between SH7760 and the power supply controller, refer to 6.2 “Serial Communications between SH7760 and the Power Supply Controller.”

6.2 Serial Communications between SH7760 and the Power Supply Controller

This section describes how serial communications take place between SH7760 and the power supply controller.

6.2.1 Serial Format

This subsection describes a format for serial communications between SH7760 and the power supply controller.

(1) Mode: Start-stop

(2) Baud rate: 38400 bits/second

(3) Stop bit: 1 bit

(4) Start bit: 1 bit

(5) Parity bit: None

(6) LSB first

6.2.2 Power Supply Control Register Read Procedure

This subsection describes a procedure for reading the power supply controller registers.

(1) SH7760 issues a read command to a power supply controller.

(2) The power supply controller returns a response to SH7760.

[Note]

(1) Don't issue multiple commands continually from SH7760. Note that the next command must be issued after a response to the preceding command has been returned from the power supply controller.

6.2.3 Read Command

Figure 6.2 shows a read command format. SH7760 sends a start code, a function code and a register address, in this order, as a read command.

(1) Start code (1 byte)	(2) Function code (1 byte or 2 byte)	(3) Register address (2byte)

Figure 6.2 Read Command

(1) Start code

The code is fixed at 0x20.

(2) Function code

• A 1-byte function code specifies the size of data to be read in the lower 4 bits when the upper 4 bits of a function code are 1000. Figure 6.3 shows a function command where the upper 4 bits are 1000.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	Size of data			

Figure 6.3 Function Command (1 Byte)

• A 2-byte function code specifies the size of data to be read in the lower 12 bits when the upper 4 bits of a function code are 1001. Figure 6.4 shows a function command where the upper 4 bits are 1001.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	Size of data											

Figure 6.4 Function Command (2 Byte)

(3) Register Address

The register address specifies the address of the register to be read

6.2.4 Normal Response during a read Operation

Figure 6.5 shows the response format for the read command. The power supply controller returns an ACK code, a function code, a register address and target data, in this order, as a response.

(1) ACK code (1 byte)	(2) Function code (1 byte or2 byte)	(3) Register address (2 byte)	(4) Data (N byte)

Figure 6.5 Normal Response during a Read Operation

(1) ACK code

This code is fixed at ACK (0x06).

(2) Function code

The same function code as for the read command returns.

(3) Register address

The address of a register subject to a read operation returns.

(4) Data

Read data returns. The size of this data is equal to the value specified in the function code.

6.2.5 Error Response during a read Operation

Figure 6.6 shows the error response format for the read command. The power supply controller returns a NAK code and an error code in this order as a response at error occurrence.

(1) NAK code (1 byte)	(2) rror code (1 byte)

Figure 6.6 Error Response during a Read Operation

(1) NAK code

This code is fixed at NAK (0x15).

(2) Error code

Table 6.1 summarizes the error codes.

Table 6.1 Error Codes

Error No	Error type
0x01	Communications error
0x02	Invalid function code
0x03	Invalid register number
0x04	Register size error
0x05	Data size error

6.2.6 Power Supply Control Register Write Procedure

This subsection describes the procedure for writing to a controller control of the power supply controller from SH7760.

(1) SH7760 issues a write command to the power supply controller.

(2) The power supply controller returns a response the SH7760.

[Note]

(1) Don't issue multiple commands continually from SH7760. Note that the next command must be issued after a response to the preceding command has been returned from the power supply controller.

6.2.7 Write Command

Figure 6.7 shows the write command format. SH7760 sends a start code, a function code, a register address and data, in this order, as a write command.

(1) Start code (1 byte)	(2) Function code (1 byte or 2 byte)	(3) Register address (2byte)	(4) Data (N byte)

Figure 6.7 Read Command

(1) Start code

This code is fixed at 0x20.

(2) Function code

• A 1-byte function code specifies the size of data to be written in the lower 4 bits when the upper 4 bits of a function code are 1100. Figure 6.3 shows a function command where the upper 4 bits are 1100.

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	Size of data			

Figure 6.8 Function Command (1 Byte)

• A 2-byte function code specifies the size of data to be written in the lower 12 bits when the upper 4 bits of a function code are 1101. Figure 6.9 shows a function command where the upper 4 bits are 1101.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	Size of data											

Figure 6.9 Function Command (2 Byte)

(3) Register Address

The register address specifies the address of the register to be written.

(4) Data

This field specifies the size of data to be written. This data size is equal to that specified in the function code.

6.2.8 Normal Response during a Write Operation

Figure 6.10 shows the response format for the write command. The power supply controller returns an ACK code, a function code, a register address and target data, in this order, as a response for the write command.

(1) ACK code (1 byte)	(2) Function code (1 byte or 2 byte)	(3) Register address (2 byte)	(4) Data (N byte)

Figure 6.10 Normal Response during a Write Operation

(1) ACK code

This code is fixed at ACK (0x06).

(2) Function code

The same code as for the write command returns.

(3) Register address

The address of a register subject to a write operation returns.

(4) Data

Write data returns. The size of this data is equal to the value specified in the function code. However, note that no data returns for IRRSFDR subject to infrared remote control and EEPDR subject to serial EEPROM control.

6.2.9 Error Response during a Write Operation

Figure 6.11 shows an error response format for the write command at error occurrence. The power supply controller returns a NAK code and an error code in this order as an error response.

(1) NAK code (1 byte)	(2) Error No. (1 byte)

Figure 6.11 Error Response during a Write Operation

(1) NAK code

This code is fixed at NAK (0x15).

(2) Error code

Table 6.2 summarizes the error codes.

Table 6.2 Error Codes

Error No	Error type
0x01	Communication error
0x02	Invalid function code
0x03	Invalid register number
0x04	Register size error
0x05	Data size error

6.3 RTC (Real-time Clock) Functions

This section describes the RTC functions. Table 6.1 summarizes the RTC registers. For detailed description of each register, refer to 6.3.1 to 6.3.17.

(1) Function for counting the seconds, minutes, hour, day of the week, month and year (BCD code)

(2) RTC start/stop function

(3) Alarm interrupt function

(4) 1sec/0.5sec cyclic interrupt function

(5) Automatic correction function for leap years

(6) Effective range of operation from January 1, 2000 to December 31, 2099

Table 6.3 RTC Registers

Register	Abbreviation	Address	R/W	Size	Remarks
RTC control register	RTCCR	0x0000	R/W	1 byte	
RTC status register	RTCSR	0x0001	R/W	1 byte	
Second counter	SECCNT	0x0002	R/W	1 byte	
Minute counter	MINCNT	0x0003	R/W	1 byte	
Hour counter	HRCNT	0x0004	R/W	1 byte	
Day-of-the-week counter	WKCNT	0x0005	R/W	1 byte	
Day counter	DAYCNT	0x0006	R/W	1 byte	
Month counter	MONCNT	0x0007	R/W	1 byte	
Year counter	YRCNT	0x0008	R/W	1 byte	
Second alarm counter	SECAR	0x0009	R/W	1 byte	
Minute alarm counter	MINAR	0x000A	R/W	1 byte	
Hour alarm counter	HRAR	0x000B	R/W	1 byte	
Day-of-the-week alarm counter	WKAR	0x000C	R/W	1 byte	
Day alarm counter	DAYAR	0x000D	R/W	1 byte	
Month alarm counter	MONAR	0x000E	R/W	1 byte	
RTC/Touch panel/Key input/Power supply status register	RTKISR	0x0090	R/W	1 byte	

6.3.1 RTC Control Register (RTCCR)

Address: 0x000, Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	CNTS	SECCAF	0.5secI	1secI	ARI	START
R	R	R/W	R/W	R/W	R/W	R/W	R/W

(1) START

START bit	Setting
0	RTC start (Initial value)
1	RTC stop

[Note]

Don't write to any counter while the START bit is set to "0." Rewrite each counter after setting the START bit to "1."

(2) ARI

ARI bit	Setting
0	No alarm interrupt is generated. (Initial value)
1	An interrupt is generated at intervals of 1 second.

(3) 1secI

1secI bit	Setting
0	No interrupt is generated at intervals of 1 second. (Initial value)
1	An interrupt is generated at intervals of 1 second.

(4) 0.5secI

0.5secI bit	Setting
0	No interrupt is generated at intervals of 0.5 second. (Initial value)
1	An interrupt is generated at intervals of 0.5 second.

(5) SECCAF

SECCAF bit	Setting
0	No carry has been generated in the second counter (SECCNT).
1	A carry has been generated in the second counter (SECCNT). [Zero-clear condition] The counter is cleared with zeros when the SECCAF bit is set to "1."

(6) CNTS

CNTS bit	Setting
0	The setting (value) of each counter is not updated. (Initial value)
1	The setting (value) of each counter is updated. [Zero-clear condition] The counter is cleared with zeros when counter update is complete. This clear operation is automatically performed.

[Note]

Don't write to any counter while the START bit is set to "0." Set the CNTS bit to "1" after updating the value of each counter with the START bit set to "1."

6.3.2 RTC Status Register (RTCSR)

Address: 0x001, Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0.5secF	1secF	ARF	0
R	R	R	R	R/W	R/W	R/W	R

(1) ARF

ARF bit	Setting
0	The setting of each alarm register with the AR bit set is not the same as that of each counter register. (Initial value)
1	The setting of each alarm register with the AR bit set is identical to that of each counter register. At this time, an interrupt occurs if the ARI bit is set to "1." [Clear condition] This counter is cleared when "0" is written with the ARF bit set to "1."

(2) 1secF

1secF bit	Setting
0	A second has not elapsed yet. (Initial value)
1	A second has elapsed. [Clear condition] This counter is cleared when "0" is written with the 1secF bit set to "1."

(3) 0.5secF

0.5secF bit	Setting
0	A half second has not elapsed yet. (Initial value)
1	A half second has elapsed. [Clear condition] This counter is cleared with zeros when "0" is written with the 0.5secF bit set to "1."

6.3.3 Second Counter (SECCNT)

Address: 0x002, Initial value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
0	10 seconds			1 second			
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The counter value is a BCD (Binary Coded Decimal) value. Counting takes place within a range from 00 to 59. When the value changes from 59 to 00, a carry is generated in the minute counter.

6.3.4 Minute Counter (MINCNT)

Address: 0z0003 Initial value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
0	10 minutes			1 minute			
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The counter value is a BCD (Binary Coded Decimal) value. Counting takes place within a range from 00 to 59. When the value changes from 59 to 00, a carry is generated in the hour counter.

6.3.5 Hour Counter (HRCNT)

Address: 0x0004, Initial value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	10 hours		1 hour			
R	R	R/W	R/W	R/W	R/W	R/W	R/W

The counter value is a BCD (Binary Coded Decimal) value. Counting takes place within a range from 00 to 59. When the value changes from 59 to 00, a carry is generated in the day counter and the day-of-the-week counter.

6.3.6 Day-of-the-Week Counter (WKCNT)

Address: 0x0005 Initial Value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	Septinary increnental counter		
R	R	R	R	R	R/W	R/W	R/W

Counting takes place within a range from 0x00 to 0x06.

- The following shows the correspondence between the day of the week and the value of the septinary incremental counter.

(D2.D1.D0) = (0.0.0) ------ Sunday
(D2.D1.D0) = (0.0.1) ------ Monday
(D2.D1.D0) = (0.1.0) ------ Tuesday
(D2.D1.D0) = (0.1.1) ------ Wednesdady
(D2.D1.D0) = (1.0.0) ------ Thursday
(D2.D1.D0) = (1.0.1) ------ Friday
(D2.D1.D0) = (1.1.0) ------ Saturday

6.3.7 Day Counter (DAYCNT)

Address: 0x0006 Initial value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	10 days		1 day			
R	R	R/W	R/W	R/W	R/W	R/W	R/W

The counter value is a BCD (Binary Coded Decimal) value. Counting takes place within a range from 1 to 31 (January, March, July, August, October and December), 1 to 30 (April, June, September and November), 1 to 28 (February in normal year) or 1 to 29 (February in leap year).

6.3.8 Month Counter (MONCNT)

Address: 0x0007 Initial value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	October	Janualy			
R	R	R	R/W	R/W	R/W	R/W	R/W

The counter value is a BCD (Binary Coded Decimal) value. Counting takes place within a range from 1 to 12. When the counter value changes from 12 to 1, a carry is generated in the year counter.

6.3.9 Year Counter (YRCNT)

Address: 0x0008 Initial value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
10 yars				1 year			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The counter value is a BCD (Binary Coded Decimal) value. Counting takes place within a range from 0 to 99. In this range, 00, 04, ..., 92 and 96 are leap years.

6.3.10 Alarm Register

Each alarm register corresponds to the relevant counter as shown below.

If the AR bit (D7) of each alarm is set to "1," counters will be compared with alarm registers. This comparison is performed only for alarm registers with the AR bit (D7) set to "1" and an alarm interrupt is generated only at correct correspondence.

• Correspondence between the alarm registers and counters

Second alarm register (BCD code): second counter

Minute alarm register (BCD code): minute counter

Hour alarm register (BCD code): Hour counter

Day-of-the-week alarm register (0x00 to 0x07): Day-of-the-week counter

Day alarm register (BCD code): Day counter

Month alarm register (BCD code): Month counter

6.3.11 Second Alarm Register (SECAR)

Address: 0x0009 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
AR	10 seconds			1 second			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The alarm value must be a BCD (Binary Coded Decimal) code between 00 and 59.

6.3.12 Minute Alarm Register (MINAR)

Address: 0x000A Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
AR	10 minutes			1 minute			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The alarm value must be a BCD (Binary Coded Decimal) code between 00 and 59.

6.3.13 Hour Alarm Register (HRAR)

Address: 0x000B Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
AR	0	10 hours		1 hour			
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

The alarm value must be a BCD (Binary Coded Decimal) code between 00 and 23.

6.3.14 Day-of-the-Week Alarm Register (WKAR)

Address: 0x000C, Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
AR	0	0	0	0	Septinary counter value		
R/W	R	R	R	R	R/W	R/W	R/W

The alarm value must be set within a range from 0x00 to 0x06.

• Day of theweek and septinary counter value
(D2.D1.D0) = (0.0.0) ------ Sunday
(D2.D1.D0) = (0.0.1) ------ Monday
(D2.D1.D0) = (0.1.0) ------ Tuesday
(D2.D1.D0) = (0.1.1) ------ Wednesdady
(D2.D1.D0) = (1.0.0) ------ Thursday
(D2.D1.D0) = (1.0.1) ------ Friday
(D2.D1.D0) = (1.1.0) ------ Saturday

6.3.15 Day Alarm Register (DAYAR)

Address: 0x000D Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
AR	0	10 days		1 day			
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

The alarm value must be a BCD (Binary Coded Decimal) code between 1 and 31 (January, March, May, July, August, October and December), between 1 and 30 (April, June, September and November), between 1 and 28 (February in normal year) or between 1 and 29 (February in leap year).

6.3.16 Month Alarm Register (MONAR)

Address: 0x000E Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
AR	0	0	October	January			
R/W	R	R	R/W	R/W	R/W	R/W	R/W

The alarm value must be a BCD (Binary Coded Decimal) code between 01 and 12.

6.3.17 RTC/Touch Panel/Key Input/Power Supply Status Register (RTKISR)

This status register indicates the RTC, touch panel or key input status. The following is a brief description of RTC-related status bits.

Address: 0x0090 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	IRRIF	POWERIF	KEYIF	TPIF	RTCIF
R	R	R	R/W	R/W	R/W	R/W	R/W

(1) RTCIF

RTCIF bit	Setting
0	The ARF, 1secF and 0.5secF bits of the RTC register are all set to “0.” (Initial value)
1	One of the ARF, 1secF ad 0.5secF bits of the RTC register is set to “1.” [Clear condition] This register is cleared when “0” is written with the RTCIF bit set to “1.”

6.4 Touch Panel Functions

This section describes the touch panel functions. In addition, Table 6.4 summarizes the touch panel registers. For details of each register, refer to 6.4.1 to 6.4.32.

(1) The A/D conversion value of the X or Y position sensed by pen touch is output.

(2) Pen touch ON/OFF interrupt function

- Sampling takes place at intervals of 20msec to 100msec. When the results (A/D conversion value of the X or Y position) obtained three times from sampling are approximate to each other, a pen touch ON interrupt is generated for SH7760. In addition, when the touch panel is turned off, a pen touch OFF interrupt is generated.

(3) To keep the pen touch "ON," sampling is performed at intervals of 20msec to 100msec and a pen touch ON interrupt is generated if the results obtained from sampling are approximate to each other.

(4) Calibration function

- Calibration is performed when two points on the touch panel are touched with the pen.
- After completion of calibration, the X and Y positions are converted into the LCD drawing dot positions for output.

Table 6.4 Touch Panel Registers

Register	Abbreviation	Address	R/W	Size	Remarks
Touch panel control register	TPLCR	0x0020	R/W	1 byte	
Touch panel status register	TPLSR	0x0021	R/W	1 byte	
Touch panel sampling control register	TPLSCR	0x0022	R/W	1 byte	
X position A/D register	XPAR	0x0024	R	2 byte	
Y position A/D register	YPAR	0x0026	R	2 byte	
X position dot register	XPDR	0x0028	R	2 byte	
Y position dot register	YPDR	0x002A	R	2 byte	
XA position dot register	XAPDR	0x002C	R/W	2 byte	
YA position dot register	YAPDR	0x002E	R/W	2 byte	
XB position dot register	XBPDR	0x0030	R/W	2 byte	
YB position dot register	YBPDR	0x0032	R/W	2 byte	
XC position dot register	XCPDR	0x0034	R/W	2 byte	
YC position dot register	YCPDR	0x0036	R/W	2 byte	
XA position A/D register	XAPAR	0x0038	R/W	2 byte	
YA position A/D register	YAPAR	0x003A	R/W	2 byte	
XB position A/D register	XBPAR	0x003C	R/W	2 byte	
YB position A/D register	YBPAR	0x003E	R/W	2 byte	
XC position A/D register	XCPAR	0x0040	R/W	2 byte	
YC position A/D register	YCPAR	0x0042	R/W	2 byte	
DX dot register	DXDR	0x0044	R/W	2 byte	
DY dot register	DYDR	0x0046	R/W	2 byte	
X position dot calculation A/D value	XPARDOT	0x0048	R/W	2 byte	
X position A/D value 1	XPARDOT1	0x004A	R/W	2 byte	
X position A/D value 2	XPARDOT2	0x004C	R/W	2 byte	
X position A/D value 3	XPARDOT3	0x004E	R/W	2 byte	
X position A/D value 4	XPARDOT4	0x0050	R/W	2 byte	
Y position dot calculation A/D value	YPARDOT	0x0052	R/W	2 byte	
Y position A/D value 1	YPARDOT1	0x0054	R/W	2 byte	
Y position A/D value 2	YPARDOT2	0x0056	R/W	2 byte	
Y position A/D value 3	YPARDOT3	0x0058	R/W	2 byte	
Y position A/D value 4	YPARDOT4	0x005A	R/W	2 byte	
RTC/Touch Panel/Key Input/Power Supply Status Register	RTKISR	0x0090	R/W	1 byte	

6.4.1 Touch Panel Control Register (TPLCR)

Address: 0x0020 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	PEN_ONRE	PEN_OFFI	PEN_ONI	TP_STR
R	R	R	R	R/W	R/W	R/W	R/W

(1) TP_STR

TP_STR bit	Setting
0	The touch panel is disabled. (Initial value)
1	The touch panel is enabled.

(2) PEN_ONI

PEN_ONI bit	Setting
0	A pen touch ON interrupt is not generated. (Initial value)
1	A pen touch ON interrupt is generated.

(3) PEN_OFFI

PEN_OFFI bit	Setting
0	A pen touch OFF interrupt is not generated. (Initial value)
1	A pen touch OFF interrupt is generated.

(4) PEN_ONRE

PEN_ ONRE bit	Setting
0	A pen touch ON interrupt is not generated when pen touch continues. (Initial value)
1	A pen touch ON interrupt is generated when pen touch continues.

6.4.2 Touch Panel Status Register (TPLSR)

Address: 0x0021 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	PEN_OFFIF	PEN_ONIF	0
R	R	R	R	R	R/W	R/W	R

(1) PEN_ONIF

PEN_ONIF bit	Setting
0	The touch panel has not been pen-touched. (Initial value)
1	The touch panel has been pen-touched. The touched positions on the touch panel are output to the X position A/D register, Y position A/D register, X position dot register and Y position dot register. At this time, a pen touch ON interrupt is generated if the PEN_ONI bit is set to "1." [Clear condition] This register is cleared when 0 is written with the PEN_ONIF bit set to "1."

(2) PEN_OFFIF

PEN_OFFIF bit	Setting
0	The touch panel has not been pen-touched (pen touch OFF). (Initial value)
1	At this time, a pen touch OFF interrupt is generated if the PEN_OFFI bit is set to "1." [Clear condition] This register is cleared when 0 is written with the PEN_OFFIF bit set to "1."

6.4.3 Touch Panel Sampling Control Register (TPLSCR)

The touch panel sampling control register sets a sampling interval for the touch panel.

Address: 0x0022 Initial value: 0x01

D7	D6	D5	D4	D3	D2	D1	D0
160msec	140msec	120msec	100msec	80msec	60msec	40msec	20msec
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

A sampling interval for the touch panel can be set within a range from 20msec to 160msec (unit: 20msec). When a bit is set to "1," the corresponding sampling interval from 20msec to 160msec is set. Note that only the following values can be specified.

• Correspondence between the setting values and sampling intervals

0x01: 20msec
0x02: 40msec
0x04: 60msec
0x08: 80msec
0x10: 100msec
0x20: 120msec
0x40: 140msec
0x80: 160msec

6.4.4 X Position A/D Register (XPAR)

Address: 0x0024 Initial value: 0x000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	XA_D11	XA_D10	XA_D9	XA_D8
R	R	R	R	R	R	R	R

D7	D6	D5	D4	D3	D2	D1	D0
XA_D7	XA_D6	XA_D5	XA_D4	XA_D3	XA_D2	XA_D1	XA_D0
R	R	R	R	R	R	R	R

The X position A/D register indicates the A/D conversion result of a pen-touched X position on the touch panel.

6.4.5 Y Position A/D Register (YPAR)

Address: 0x0026 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	YA_D11	YA_D10	YA_D9	YA_D8
R	R	R	R	R	R	R	R

D7	D6	D5	D4	D3	D2	D1	D0
YA_D7	YA_D6	YA_D5	YA_D4	YA_D3	YA_D2	YA_D1	YA_D0
R	R	R	R	R	R	R	R

The Y position A/D register indicates the A/D conversion result of a pen-touched Y position on the touch panel.

6.4.6 X Position Dot Register (XPDR)

Address: 0x0028 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
XD_D15	XD_D14	XD_D13	XD_D12	XD_D11	XD_D10	XD_D9	XD_D8
R	R	R	R	R	R	R	R

D7	D6	D5	D4	D3	D2	D1	D0
XD_D7	XD_D6	XD_D5	XD_D4	XD_D3	XD_D2	XD_D1	XD_D0
R	R	R	R	R	R	R	R

The X position dot register indicates the dot position of a pen-touched X position on the touch panel. Use the output value of this register after calibration. The output value is not settled without calibration.

6.4.7 Y Position Dot Register (YPDR)

Address: 0x002A Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
YD_D15	YD_D14	YD_D13	YD_D12	YD_D11	YD_D10	YD_D9	YD_D8
R	R	R	R	R	R	R	R

D7	D6	D5	D4	D3	D2	D1	D0
YD_D7	YD_D6	YD_D5	YD_D4	YD_D3	YD_D2	YD_D1	YD_D0
R	R	R	R	R	R	R	R

The Y position dot register indicates the dot position of a pen-touched Y position on the touch panel. Use the output value of this register after calibration. The output value is not settled without calibration.

6.4.8 XA Position Dot Register (XAPDR)

Address: 0x002C Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
XAD_D15	XAD_D14	XAD_D13	XAD_D12	XAD_D11	XAD_D10	XAD_D9	XAD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XAD_D7	XAD_D6	XAD_D5	XAD_D4	XAD_D3	XAD_D2	XAD_D1	XAD_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The XA position dot register indicates the X dot position of point A when calibration takes place.

6.4.9 YA Position Dot Register (YAPDR)

Address: 0x002E Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
YAD_D15	YAD_D14	YAD_D13	YAD_D12	YAD_D11	YAD_D10	YAD_D9	YAD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YAD_D7	YAD_D6	YAD_D5	YAD_D4	YAD_D3	YAD_D2	YAD_D1	YAD_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The YA position dot register indicates the Y dot position of point A when calibration takes place.

6.4.10 XB Position Dot Register (XBPDR)

Address: 0x0030 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
XBD_D15	XBD_D14	XBD_D13	XBD_D12	XBD_D11	XBD_D10	XBD_D9	XBD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XBD_D7	XBD_D6	XBD_D5	XBD_D4	XBD_D3	XBD_D2	XBD_D1	XBD_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The XB position dot register indicates the X dot position of point B when calibration takes place.

6.4.11 YB Position Dot Register (YBPDR)

Address: 0x0032 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
YBD_D15	YBD_D14	YBD_D13	YBD_D12	YBD_D11	YBD_D10	YBD_D9	YBD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YBD_D7	YBD_D6	YBD_D5	YBD_D4	YBD_D3	YBD_D2	YBD_D1	YBD_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The YB position dot register indicates the Y dot position of point B when calibration takes place.

6.4.12 XC Position Dot Register (XCPDR)

Address: 0x0034 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
XCD_D15	XCD_D14	XCD_D13	XCD_D12	XCD_D11	XCD_D10	XCD_D9	XCD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XCD_D7	XCD_D6	XCD_D5	XCD_D4	XCD_D3	XCD_D2	XCD_D1	XCD_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The XC position dot register indicates the X dot position of point C when calibration takes place. This register will be functionally enhanced in future. Don't access this register.

6.4.13 YC Position Dot Register (YCPDR)

Address: 0x0036 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
YCD_D15	YCD_D14	YCD_D13	YCD_D12	YCD_D11	YCD_D10	YCD_D9	YCD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YCD_D7	YCD_D6	YCD_D5	YCD_D4	YCD_D3	YCD_D2	YCD_D1	YCD_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The YC position dot register indicates the Y dot position of point C where calibration takes place. This register will be functionally enhanced in future. Don't access this register.

6.4.14 XA Position A/D Register (XAPAR)

Address: 0x0038 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	XAA_D11	XAA_D10	XAA_D9	XAA_D8
R	R	R	R	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XAA_D7	XAA_D6	XAA_D5	XAA_D4	XAA_D3	XAA_D2	XAA_D1	XAA_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The XA position A/D register indicates the X position A/D conversion result of point A subject to calibration/

6.4.15 YA Position A/D Register (YAPAR)

Address: 0x003A Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	YAA_D11	YAA_D10	YAA_D9	YAA_D8
R	R	R	R	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YAA_D7	YAA_D6	YAA_D5	YAA_D4	YAA_D3	YAA_D2	YAA_D1	YAA_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The YA position A/D register indicates the Y position A/D conversion result of point A subject to calibration

6.4.16 XB Position A/D Register (XBPAR)

Address: 0x003C Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	XBA_D11	XBA_D10	XBA_D9	XBA_D8
R	R	R	R	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XBA_D7	XBA_D6	XBA_D5	XBA_D4	XBA_D3	XBA_D2	XBA_D1	XBA_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The XB position A/D register indicates the X position A/D conversion result of point B subject to calibration.

6.4.17 YB Position A/D Register (YBPAR)

Address: 0x003E Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	YBA_D11	YBA_D10	YBA_D9	YBA_D8
R	R	R	R	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YBA_D7	YBA_D6	YBA_D5	YBA_D4	YBA_D3	YBA_D2	YBA_D1	YBA_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The YB position A/D register indicates the Y position A/D conversion result of point B subject to calibration.

6.4.18 XC Position A/D Register (XCPAR)

Address: 0x0040 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	XCA_D11	XCA_D10	XCA_D9	XCA_D8
R	R	R	R	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XCA_D7	XCA_D6	XCA_D5	XCA_D4	XCA_D3	XCA_D2	XCA_D1	XCA_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The XC position A/D register indicates the X position A/D conversion result of point C subject to calibration. This register will be functionally enhanced in future. Don't access this register.

6.4.19 YC Position A/D Register (YCPAR)

Address: 0x0042 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	YCA_D11	YCA_D10	YCA_D9	YCA_D8
R	R	R	R	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YCA_D7	YCA_D6	YCA_D5	YCA_D4	YCA_D3	YCA_D2	YCA_D1	YCA_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The YC position A/D register indicates the Y position A/D conversion result of point C subject to calibration. This register will be functionally enhanced in future. Don't access this register

6.4.20 DX Dot Register (DXDR)

Address: 0x0044 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
DX1_D15	DX1_D14	DX1_D13	DX1_D12	DX1_D11	DX1_D10	DX1_D9	DX1_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
DX1_D7	DX1_D6	DX1_D5	DX1_D4	DX1_D3	DX1_D2	DX1_D1	DX1_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The DX dot register holds a value obtained by multiplying the number of dots per data (X position A/D conversion result at calibration) by 1,000. The power supply controller outputs a dot position of the X position to be stored in the X position dot register (XPDR) from the values set in the DX dot register (DXDR), XA position dot register (XAPDR) and XA position A/D register (XAPAR). When the DX dot register (DXDR) has been set to "0," the dot position is not calculated.

6.4.21 DY Dot Register (DYDR)

Address: 0x0046 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
DY1_D15	DY1_D14	DY1_D13	DY1_D12	DY1_D11	DY1_D10	DY1_D9	DY1_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
DY1_D7	DY1_D6	DY1_D5	DY1_D4	DY1_D3	DY1_D2	DY1_D1	DY1_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The DY dot register (DY1DR) holds a value obtained by multiplying the number of dots per data (Y position A/D conversion result at calibration) by 1,000. The power supply controller outputs a dot position of the Y position to be stored in the Y position dot register (YPDR) from the values set in the DY dot register (DYDR), YA position dot register (YAPDR) and YA position A/D register (YAPAR). When the DY dot register (DY1DR) has been set to "0," the dot position is not calculated.

6.4.22 X Position Dot Calculation A/D Value (XPARDOT)

Address: 0X0048 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	XD_D9	XD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XD_D7	XD_D6	XD_D5	XD_D4	XD_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The X position dot calculation A/D value register (XPARDOT) holds an AD value of X position dot calculation. This A/D value is obtained by calculating the mean of the previous four XPARDOT values and clearing the low order 3 bits with zeros.

6.4.23 X Position Dot Calculation A/D Value 1 (XPARDOT1)

Address: 0x004A Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	XD1_D9	XD1_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XD1_D7	XD1_D6	XD1_D5	XD1_D4	XD1_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The X position dot calculation A/D value 1 register (XPARDOT1) holds an XPARDOT value before sampling.

6.4.24 X Position Dot Calculation A/D Value 2 (XPARDOT2)

Address: 0x004C Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	XD2_D9	XD2_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XD2_D7	XD2_D6	XD2_D5	XD2_D4	XD2_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The X position dot calculation A/D value 2 register (XPARDOT2) holds an XPARDOT value before sampling.

6.4.25 X Position Dot Calculation A/D Value 3 (XPARDOT3)

Address: 0x004E Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	XD3_D9	XD3_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XD3_D7	XD3_D6	XD3_D5	XD3_D4	XD3_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The X position dot calculation A/D value 3 register (XPARDOT3) holds an XPARDOT value before sampling.

6.4.26 X Position Dot Calculation A/D Value 4 (XPARDOT4)

Address: 0x0050 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	XD4_D9	XD4_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XD4_D7	XD4_D6	XD4_D5	XD4_D4	XD4_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The X position dot calculation A/D value 4 register (XPARDOT4) holds an XPARDOT value before sampling.

6.4.27 Y Position Dot Calculation A/D Value (YPARDOT)

Address: 0x0052 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	YD_D9	YD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YD_D7	YD_D6	YD_D5	YD_D4	YD_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The Y position dot calculation A/D value register (YPARDOT) holds an A/D value of Y position dot calculation. This A/D value is obtained by calculating the mean of the previous four YPARDOT values and clearing the following 3 bits with zeros.

6.4.28 Y Position Dot Calculation A/D Value 1 (YPARDOT1)

Address: 0 x0054 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	YD1_D9	YD1_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YD1_D7	YD1_D6	YD1_D5	YD1_D4	YD1_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The Y position dot calculation A/D value 1 register (YPARDOT1) holds a YPARDOT value before sampling.

6.4.29 Y Position Dot Calculation A/D Value 2 (YPARDOT2)

Address: 0x0056 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	YD2_D9	YD2_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YD2_D7	YD2_D6	YD2_D5	YD2_D4	YD2_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The Y position dot calculation A/D value 2 register (YPARDOT2) holds a YPARDOT value before sampling

6.4.30 Y Position Dot Calculation A/D Value 3 (YPARDOT3)

Address: 0x0058 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	YD3_D9	YD3_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YD3_D7	YD3_D6	YD3_D5	YD3_D4	YD3_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The Y position dot calculation A/D value 3 register (YPARDOT3) holds a YPARDOT value before sampling.

6.4.31 Y Position Dot Calculation A/D Value 4 (YPARDOT4)

Address: 0x005A Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	YD4_D9	YD4_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YD4_D7	YD4_D6	YD4_D5	YD4_D4	YD4_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The Y position dot calculation A/D value 4 register (YPARDOT4) holds a YPARDOT value before sampling.

6.4.32 RTC/Touch Panel/Key Input/Power Supply Status Register (RTKISR)

This status register indicates the RTC, touch panel, or key input status. Below is a brief description of the status bits related to the touch panel.

Address: 0x0090 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	IRRIF	POWERIF	KEYIF	TPIF	RTCIF
R	R	R	R/W	R/W	R/W	R/W	R/W

(1) TPIF

TPIF bit	Setting
0	The PEN_ONIF, PEN_OFFIF, CAIF and CAEF bits of the touch panel status registered are all set to “0.” (Initial value)
1	One of the PEN_ONIF, PEN_OFFIF, CAIF and CAEF bits of the touch panel status register is set to “1.” [Clear condition] This bit is cleared when “0” is written with the TPIF bit set to “1.”

6.4.33 Touch Panel Calibration Method (2-point System)

The power supply controller supports 2-point touch panel calibration. Figure 6.11shows the points of the drawing coordinates and A/D conversion coordinates that are necessary for calibration.

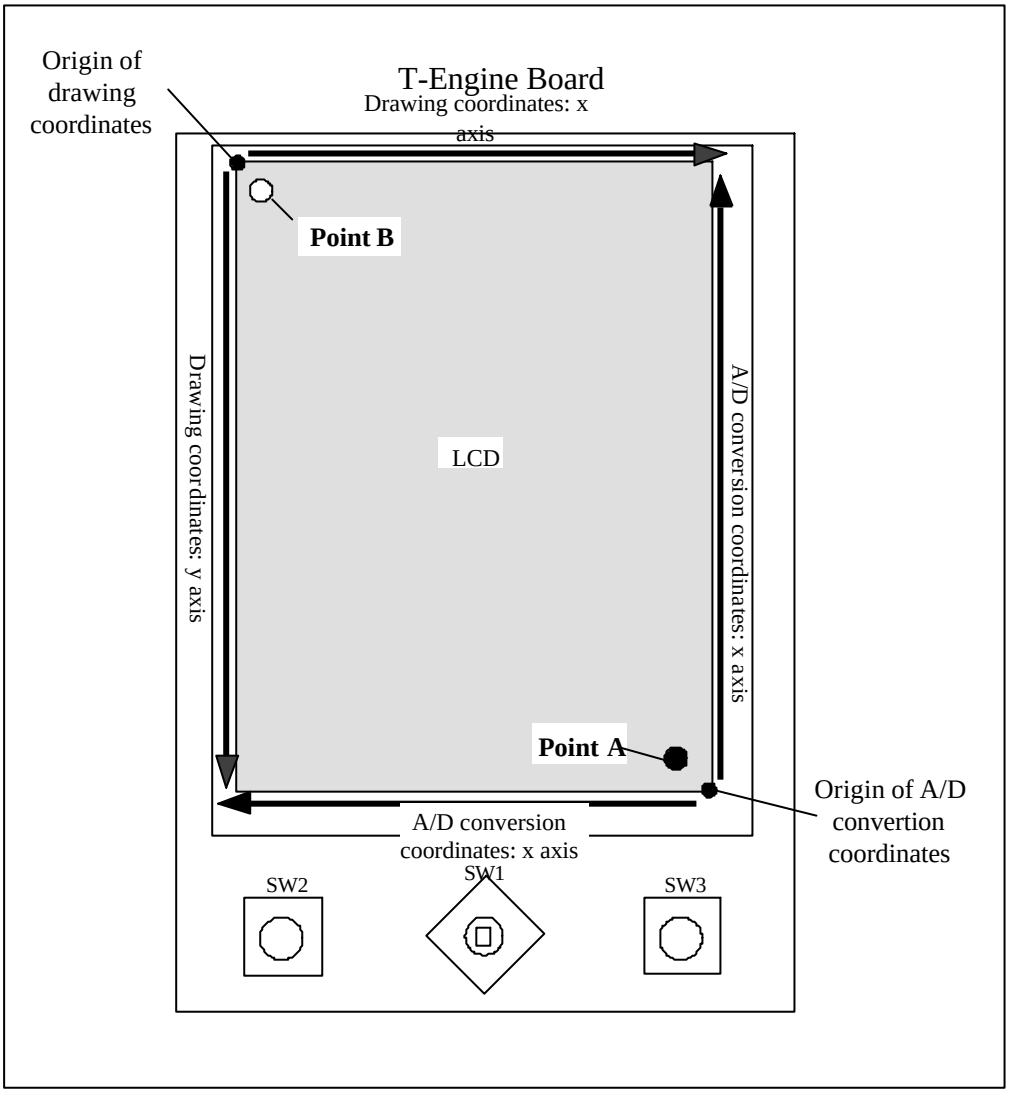


Figure 6.11 Points of the Drawing Coordinates and A/D Conversion Coordinates

[Calibration Method]

(1) The SH7760 writes the dot points of points A and B to the registers XAPDR, YAPDR, XBPDR, and YBPDR.

(2) When point A is pen-touched, it is signaled by a pen touch interrupt. The A/D conversion result of the pen-touched point A is written to the registers XAPAR and YAPAR.

(3) Next, when point B is pen-touched, it is signaled by a pen touch interrupt. The A/D conversion result of the pen-touched point B is written to the registers XBPAR and YBPAR.

(4) Calibration takes place according to data in the above steps (1) to (3). Using the following expression, the SH7760 calculates the number of dots per data of the X position A/D conversion result and that of the Y position A/D conversion result.

Number of dots per data of the X position A/D conversion result (DX)
DX = (DXA – DXB) / (TXB – TXA) Where TXA < TXB, DXA > DXB
Number of dots per data of the Y position A/D conversion result (DY)
DY = (DYA – DYB) / (TYB- TYA) Where TYA < TYB, DYA > DYB

DXA: X position drawing dot point of point A (XAPDR)
DXB: X position drawing dot point of point B (XBPDR)
TXA: X position A/D conversion result of point A (XAPAR)
TXB: X position A/D conversion result of point B (XBPAR)
DYA: Y position drawing dot point of point A (YAPDR)
DYB: Y position drawing dot point of point B (YBPDR)
TXA: Y position A/D conversion result of point A (YAPAR)
TXB: Y position A/D conversion result of point B (YBPAR)

(5) The above calculation results are multiplied by 1,000, their decimal places are rounded, and the resulting integers are written to the registers DXDR and DYDR.

DX dot register (DXDR) = DX x 1,000 (rounding the decimal places)
DY dot register (DYDR) = DY x 1,000 (rounding the decimal places)

(6) The power supply controller uses data stored in the registers DXDR, DYDR, XAPDR, YAPDR, XAPAR, and YAPAR to calculate dot position data (XPDR, YPDR) of the pen-touched point on the LCD. The power supply controller uses the following expression to calculate dot position data.

X position dot register (XPDR)
XPDR = (DXA – (DX x (TXD – TXA)) / 1,000
Y position dot register (YPDR)
YPDR = (DYA – (DY x (TYD – TYA)) / 1,000
DXA: XA position dot register (XAPDR) data
DX: DX1 dot register (DXDR) data
TXA: XA position A/D register (XAPAR) data
TXD: X position A/D register (XPAR) data
DYA: YA position dot register (YAPDR) data
DY: DY dot register (DYDR) data
TYA: YA position A/D register (YAPAR) data
TYD: X position A/D register (YPAR) data

The power supply controller outputs data stored in the X position A/D register (XPAR) and Y position A/D register (YPAR). When the values stored in the DX dot register (DXDR) and DY dot register (DYDR) are not 0, the power supply controller outputs the data derived from the above expressions to the X position dot register (XPDR) and Y position dot register (YPDR). When either value is 0, it does not use the above expression for calculation and outputs only XPAR and YPAR data.

6.5 Key Switch Control

Figure 6.12 shows the Solution Engine2 switches under control by the power supply controller. The power supply controller controls the switches SW1 to SW3 on the CPU board and the switches SW1to SW3 on the LCD board.

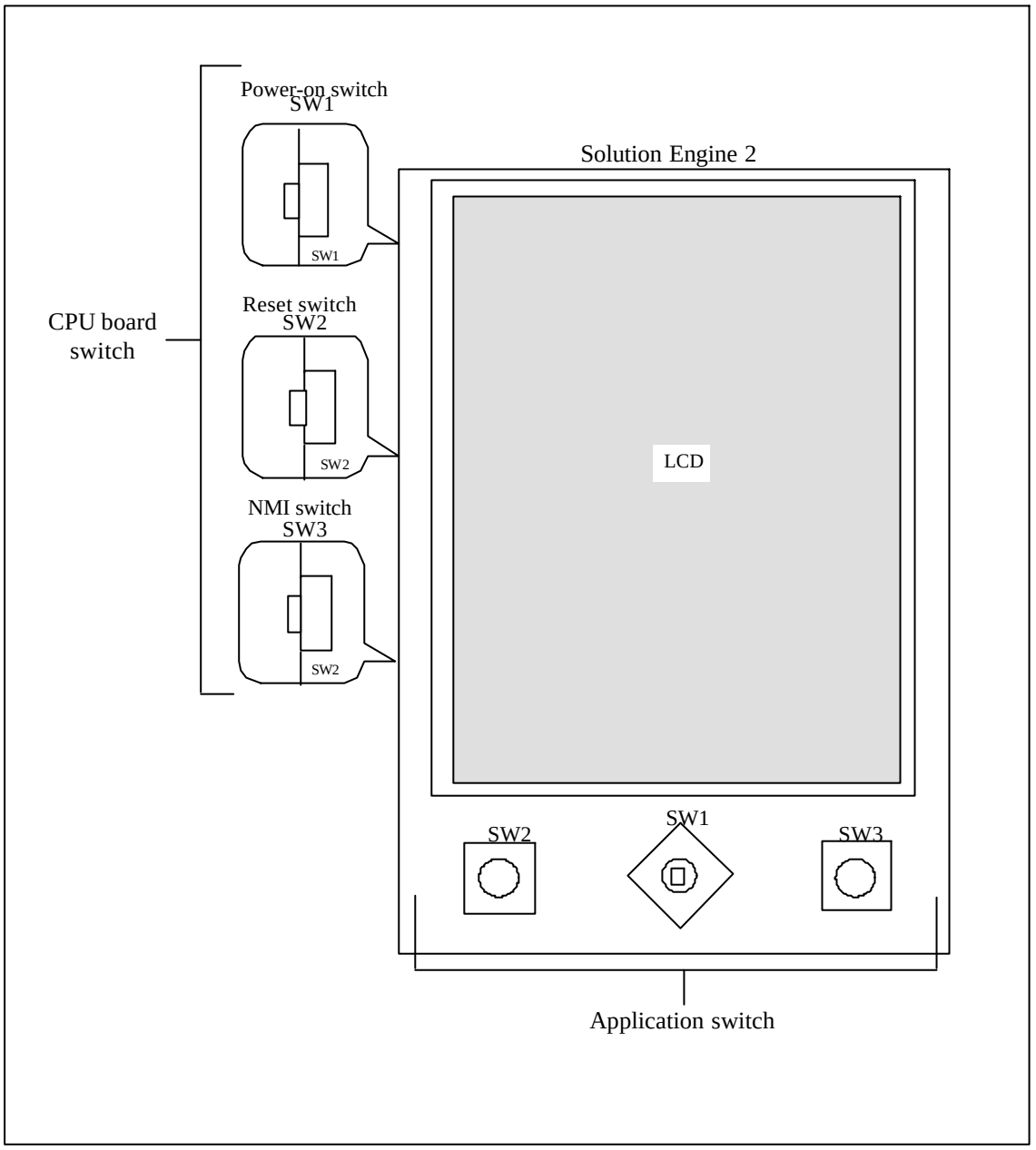


Figure 6.12 Solution Engine 2 Switch

6.5.1 CPU Board Switch Control

(1) Power-on switch (SW1)

- When the SH7760 is being powered, a power-on switch interrupt occurs for the SH7760 if the power-on switch is pressed and held for 2 seconds or more.
- When Solution Engine2 is OFF, it is turned ON if the power-on switch is pressed and held for 0.5 seconds or more.
- When Solution Engine2 is ON, it is turned OFF if the power-on switch is pressed and held for 2 seconds or more.

(2) Reset switch (SW2)

Solution Engine2 is turned OFF when the reset switch is pressed.

(3) NMI switch (SW3)

An NMI interrupt occurs for the SH7760 when the NMI switch is pressed.

6.5.2 LCD Board Switch Control (Application Switch)

(1) Cursor switch (SW1) and push-button switches (SW2 and SW3) on the LCD board

- The cursor switch and push-button switches are subject to sampling at intervals of 10msec. When consecutive three samplings indicate that the same key is being pressed, key bit pattern data of the cursor switch and push-button switches are output.
- If the switch is turned ON, a key ON interrupt occurs. If the switch is turned OFF, a key OFF interrupt occurs.
- When the same switch is pressed and held, an auto repeat interrupt occurs at intervals of 100 to 450msec (unit: 50msec).

6.5.3 Key Switch Registers

Table 6.5 summarizes the key switch registers. For details of each register, refer to 6.5.4 to 6.5.8.

Table 6.5 Key Switch Registers

Register	Abbreviation	Address	R/W	Size	Remarks
Key control register	KEYCR	0x0060	R/W	1 byte	
Key auto repeat time register	KATIMER	0x0061	R/W	1 byte	
Key input status register	KEYSR	0x0062	R/W	1 byte	
Key bit pattern register	KBITPR	0x0064	R/W	2 byte	
RTC/Touch panel/Key input/Power supply status register	RTKISR	0x0090	R/W	1 byte	

6.5.4 Key Control Register (KEYCR)

Address: 0x0060 Initial value: 0x20

D7	D6	D5	D4	D3	D2	D1	D0
0	0	NMIE	PONSWI	ARKEYI	KEY_OFFI	KEY_ONI	KEY_STR
R	R	R/W	R/W	R/W	R/W	R/W	R/W

(1) KEY_STR

KEY_STR bit	Setting
0	An application switch key input is disabled. (Initial value)
1	An application switch key input is enabled.

(2) KEY_ONI

KEY_ONI bit	Setting
0	An application switch ON interrupt is disabled. (Initial value)
1	An application switch key ON interrupt is enabled.

(3) KEY_OFFI

KEY_OFFI bit	Setting
0	An application switch OFF interrupt is disabled. (Initial value)
1	An application switch key OFF interrupt is enabled.

(4) ARKEY

ARKEY bit	Setting
0	An application switch auto repeat interrupt is disabled. (Initial value)
1	An application switch auto repeat interrupt is enabled.

(5) PONSWI

PONSWI bit	Setting
0	A power-on switch interrupt is disabled. (Initial value)
1	A power-on switch interrupt is enabled.

(6) NMIE

NMIE bit	Setting
0	An NMI interrupt is disabled for the SH7760 even when the NMI switch is pressed.
1	An NMI interrupt is enabled for the SH7760 when the NMI switch is pressed. (Initial value)

6.5.5 Key Auto Repeat Time Register (KATIMER)

Address: 0x0061 Initial value: 0x01

D7	D6	D5	D4	D3	D2	D1	D0
450msec	400msec	350msec	300msec	250msec	200msec	150msec	100msec
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register sets the auto repeat interrupt generation time. The auto repeat interrupt generation time is set at intervals of 100msec to 450msec (unit: 50msec). When one of the bits (100msec to 450msec) is set, the corresponding auto repeat interrupt generation time is set.

6.5.6 Key Bit Pattern Register (KBIPR)

Address: 0x0064 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	SW2	0	SW3
R	R	R	R	R	R	R	R

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	SW1-5 (Decided)	SW1-4 (↓)	SW1-3 (↑)	SW1-2 (←)	SW1-1 (→)
R	R	R	R	R	R	R	R

This register stores the bit pattern of the application switch (SW1 to SW3) key input status.

(1) SWn

SWn bit	Setting
0	Application switch key input: OFF (Initial value)
1	Application switch key input: ON

6.5.7 Key Input Status Register (KEYSR)

Address: 0x0062 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	PONSWF	ARKEYF	KEY_OFFF	KEY_ONF	0
R	R	R	R/W	R/W	R/W	R/W	R

(1) KEY_ONF

KEY_ON bit	Setting
0	An application switch key has not been turned on. (Initial value)
1	An application switch key has been turned on. At this time, if the KEY_ONI bit is set to "1," a key ON interrupt occurs. [Clear condition] This bit is reset when "0" is written with the KEY_ONF bit set to "1."

(2) KEY_OFFF

KEY_OFFF bit	Setting
0	An application switch key is ON or OFF. (Initial value)
1	An application switch key has changed from ON to OFF. (Initial value) At this time, if the KEY_OFFI bit is set to "1," a key OFF interrupt occurs. [Clear condition] This bit is cleared when "0" is written with the KEY_OFFI bit set to "1."

(3) ARKEYF

ARKEYF bit	Setting
0	The same application switch key is not ON for the time specified in the key auto repeat time register. (Initial value)
1	The same application switch is ON for the time specified in the key auto repeat time register. At this time, if the ARKEYI bit is set to "1"," repeat interrupt occurs. [Clear condition] This bit is cleared when "0" is written with the ARKEYF bit set to "1."

(4) PONSWF

PONSWF bit	Seeting
0	The power-on switch has not been turned on for 2sec or more.
1	The power-on switch has been turned on for 2 sec or more. At this time, if the PONSWI bit is set to “1,” a power-on interrupt occurs. [Clear condition] This bit is cleared when “0” is written to the PONSWF bit set to “1.”

[Supplementary description on application switch key input]

(1) When multiple keys are pressed at the same time, the corresponding bits are all set to “1,” and a KEY_ONF interrupt occurs so long as it is enabled.

(2) If data in the key bit pattern register changes when multiple keys are pressed at the same time, a KEY_ONF interrupt occurs so long as it is enabled.

- Example -

This KEY_ONF interrupt occurs when the state with switches SW1 and SW2 pressed simultaneously changes to one with switches SW1 and SW3 pressed simultaneously.

(3) When multiple keys are released in the state with the keys pressed and held, a KEY_OFFI interrupt occurs so long as it is enabled.

(4) When multiple keys are released, the key states immediately before key release are retained in the key bit pattern register.

6.5.8 RTC/Touch Panel/Key Input/Power Supply Status Register (RTKISR)

This status register indicates the RTC, touch panel, or key input status. Below is a brief description of the status bits for key input.

Address: 0x0090 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	IRRIF	POWERIF	KEYIF	TPIF	RTCIF
R	R	R	R/W	R/W	R/W	R/W	R/W

(1) KEYIF

KEYIF bit	Setting
0	The PONSWF, ARKEYF, KEY_OFFF, and KEY_ONF bits of the key input status register are all set to “0.” (Initial value)
1	One of the PONSWF, ARKEYF, KEY_OFFF, or KEY_ONF bits of the key input status register is set to “1.” [Clear condition] This bit is cleared when “0” is written with the KEYIF bit set to “1.”

6.6 Power Supply Control

This section describes the power supply control functions. Table 6.6 summarizes the power supply controller registers. In addition, refer to 6.6.1 to 6.6.3 for details of each register.

(1) Solution Engine2 is turned ON or OFF.

(2) When Solution Engine2 is OFF, it is turned ON if the power-on switch is pressed for 2sec or more.

(3) Solution Engine2 can be turned OFF from the SH7760.

(4) If the DIP switch (SW7) is se to ON, Solution Engine2 is also turned ON at the same time the power supply controller is turned ON.

Table 6.6 Power Control Registers

Register	Abbreviation	Address	R/W	Size	Remarks
System power control register 1	SPOWCR1	0x0070	R/W	1 byte	
System power control register 2	SPOWCR2	0x0071	R/W	1 byte	

6.6.1 System Power Control Register 1 (SPOWCR1)

Address: 0x0070 Initial value: 0x01

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	SPOWER
R	R	R	R	R	R	R	R/W

(1) SPOWER

SPOWER bit	Setting
0	System power supply: OFF
1	System power supply: ON (Initial value)

6.6.2 System Power Control Register 2 (SPOWCR2)

Address: 0x0071 Initial value: 0x01

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	SFPOWER
R	R	R	R	R	R	R	R/W

(2) SFPOWER

SFPOWER	Setting
0	Solution Engine2 is turned OFF by SH7760 control.
1	Solution Engine2 is turned OFF by pressing the power-on switch. (Initial value)

6.6.3 RTC/Touch Panel/Key Input/Power Supply Status Register (RTKISR)

This status register indicates the RTC, touch panel, or key input status. Below is a brief description of the status bits for power control.

Address: 0x0090 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	IRRIF	POWERIF	KEYIF	TPIF	RTCIF
R	R	R	R/W	R/W	R/W	R/W	R/W

(1) POWERIF

This bit will be functionally enhanced in the future. Don't access this register. When read, this bit is always 20."

6.7 LED Control

This section describes the LED control functions. Table 6.7 summarizes the LED controller registers. Though SH7760 Solution Engine2 has not been provided with LED1 to LED8, LED control is executed.

(1) Controlling the ON/OFF State of LEDs (LED1 to LED8) on the CPU board

Table 6.7 LED Controller Registers

Register	Abbreviation	Address	R/W	Size	Remarks
LED register	LEDR	0x00A0	R/W	1byte	

6.7.1 LED Register (LEDR)

Address: 0x00A0 Initial value: 0xXX

D7	D6	D5	D4	D3	D2	D1	D0
LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

(1) LEDn

LEDn bit	Setting
0	LEDn is turned OFF.
1	LEDn is turned ON.

LEDn is turned ON for the H8/3048F-ONE firmware version at the power-on sequence.

6.8 LCD Front Light Control

This section describes the LCD light control functions. In addition, Table 6.8 summarizes the front light control registers.

(1) Controlling the ON/OFF state of the LCD front light

Table 6.8 LCD Front Light Registers

Register	Abbreviation	Address	R/W	Size	Remarks
LCD front light registers	LCDR	0x00A1	R/W	1byte	

6.8.1 LCD Front Light Register (LCDR)

Address: 0x00A1 Initial value: 0x01

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	FRONTL
R	R	R	R	R	R	R	R/W

(1) FRONTL

FRONTL bit	Setting
0	The LCD front light is turned ON.
1	The LCD front light is turned OFF (Initial value)

6.9 Reset Control

This section describes the reset control functions. Table 6.9 summarizes the reset control registers.

(1) Solution Engine2 reset is controlled.

Table 6.9 Reset Registers

Register	Abbreviation	Address	R/W	Size	Remarks
Reset control register	RESTCR	0x00A2	R/W	1 byte	

6.9.1 RESTCR Register (RESTCR)

Address: 0x00A2 Initial value: 0x02

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	SWRES	SORES
R	R	R	R	R	R	R/W	R/W

(1) SORES

SORES bit	Setting
0	Solution Engine2 is not restarted by reset. (Initial value)
1	Solution Engine2 is restarted by reset.

If this bit is set to “1,” Solution Engine2 is restarted.

(2) SWRES

SWRES bit	Setting
0	Devices other than the power supply controller are reset with the reset switch (SW2).
1	All the devices covering the power supply controller are reset with the reset switch (SW2). (Initial value)

6.10 Infrared Remote Control

This section describes the infrared remote control functions. Table 6.10 summarizes the infrared remote control functions. For details of each register, refer to 6.10.1 to 6.10.8.

(1) Support of formats for two kinds of infrared remote control signal

Supported format: NEC format and Home Appliance Manufacturer's Association format

(2) Function for receiving infrared remote control signals

- A maximum of 255 bytes of the infrared remote control signal can be stored. Receive data can be read from the receiving FIFO data register (IRRRFDR).
- Infrared remote control signals of a specified format can be received.
- When a frame signal has been received, a receiving interrupt may be generated.

(3) Function for transmitting infrared remote control signals

- A maximum of 255 bytes of the infrared remote control signal can be transmitted.
- Transmit data can be written to the transmitting FOFOI data register (IRRSFDR).
- Infrared remote control signals of the specified format are transmitted.

Table 6.10 Infrared Remote Control Registers

Register	Abbreviation	Address	R/W	Size
Infrared remote control register	IRRCR	0x00B0	R/W	1 byte
Infrared remote control status register	IRRSR	0x00B1	R/W	1 byte
Receive data count register for infrared remote control signals	IRRRDNR	0x00B2	R	1 byte
Transmit data count register for infrared remote control signals	IRRSDNR	0x00B3	R	1 byte
Receive FIFO data register for infrared remote control signals	IRRRFDR	0x00B4	R	1 byte
Transmit FIFO data register for infrared remote control signals	IRRSFDR	0x00B5	W	1 byte

6.10.1 Infrared Remote Control Register (IRRCR)

Address; 0x00B0 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	TDIE	RDIE	FORMAT	START
R	R	R	R	R/W	R/W	R/W	R/W

(1) START

START bit	Setting
0	Infrared remote control is disabled. (Initial value)
1	Infrared remote control is enabled to start data transmission/reception.

(2) FORMAT

FORMAT bit	Setting
0	The NEC format is set, (Initial value)
1	The Home Appliance Manufacturer's Association format is set

(3) RDIE

RDIE bit	Setting
0	An interrupt is disabled upon completion of receiving a frame of infrared remote control signal. (Initial value).
1	An interrupt is enabled upon completion of receiving a frame of infrared remote control signal.

(4) TDIE

TDIE bit	Setting
0	An interrupt is disabled upon completion of transmitting a frame of infrared remote control signal. (Initial value)
1	An interrupt is enabled upon completion of transmitting a frame of infrared remote control signal.

6.10.2 Infrared Remote Control Status Register (IRRSR)

Address: 0x00B1 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	TDI	RDI	0	RDBFER
R	R	R	R	R/W	R/W	R	R/W

(1) RDBFER

RDBFER bit	Setting
0	A buffer full error has not occurred during a receive operation. (Initial value)
1	A buffer full error has occurred during a receive operation.

(2) RDI

RDI bit	Setting
0	A frame of data has not been received. (Initial value)
1	A frame of data has been received. [Clear condition] This bit is cleared when “0” is written with the RDI bit set to “1.”

(3) TDI

TDI bit	Setting
0	A frame of data has not been transmitted. (Initial value)
1	A frame of data has been transmitted. [Clear condition] This bit is cleared when “0” is written with the TDI bit set to “1.”

6.10.3 Receive Data Count Register for Infrared Remote Control Signals (IRRRDNR)

Address: 0x00B2 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
IRRRD_D7	IRRRD_D6	IRRRD_D5	IRRRD_D4	IRRRD_D3	IRRRD_D2	IRRRD_D1	IRRRD_D0
R	R	R	R	R	R	R	R

This register indicates the number of received data items (infrared remote control signals) stored in the receive FIFO register. When this register is "0x00," it indicates that there is no data. When the value of this register is "0xFF," it indicates that the receive FIFO register is full of data.

6.10.4 Transmit Data Count Register for Infrared Remote Control Signals

Address: 0x00B3 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
IRRSD_D7	IRRSD_D6	IRRSD_D5	IRRSD_D4	IRRSD_D3	IRRSD_D2	IRRSD_D1	IRRSD_D0
R	R	R	R	R	R	R	R

This register indicates the number of data items not transmitted (infrared remote control signals) stored in the transmit FIFO register. When the value of this register is "0x00," it indicates that there is no data. When the value of this register is "0xFF," it indicates that the transmit FIFO buffer is full of data.

6.10.5 Receiving the FIFO Data Register for Infrared Remote Control Signals (IRRRFDR)

Address: 0x00B4 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
IRRRDR_D7	IRRRDR_D6	IRRRDR_D5	IRRRDR_D4	IRRRDR_D3	IRRRDR_D2	IRRRDR_D1	IRRRDR_D0
R	R	R	R	R	R	R	R

This register is an 8-bit FIFO register for storing received data. All the received data can be obtained from this register until it is emptied. For details, refer to 6.1.8, "Infrared Remote Control Data Structure."

6.10.6 Transmitting the FIFO Data Register for Infrared Remote Control Signals (IRRSFDR)

Address: 0x00B5 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
IRRSDR_D7	IRRSDR_D6	IRRSDR_D5	IRRSDR_D4	IRRSDR_D3	IRRSDR_D2	IRRSDR_D1	IRRSDR_D0
W	W	W	W	W	W	W	W

This register is an 8-bit FIFO register that stores transmission data. Transmission data can be stored until this register is filled with data. For details, refer to 6.10.8, "Infrared Remote Control Data Structure."

6.10.7 RTC/Touch Panel/Key Input/Power Supply Status Register (RTKISDR)

This status register indicates the RTC, touch panel, or key input status. Below is a brief description of the status bits for infrared remote control signals.

Address: 0x0090 Initial value: 0x00

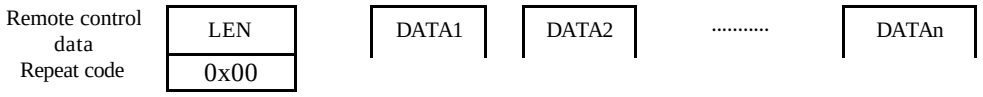
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	IRRIF	POWERIF	KEYIF	TPIF	RTCIF
R	R	R	R/W	R/W	R/W	R/W	R/W

(1) IRRIF

IRRIF bit	Setting
0	A frame of data has not been transmitted or received. (Initial value)
1	A frame of data has been transmitted or received. [Clear condition] This bit is cleared when "0" is written with the IRRI bit set to "1."

6.10.8 Infrared Remote Control Data Structure

The following shows the relation between the infrared remote control data and repeat codes. In addition, it shows a structure of remote control data in the NEC format.



Example) NEC format remote control data

[Infrared Remote Control Operation Procedure]

[Initial setting]

(1) Two kinds of formats are set by selecting the FORMAT bit of the IRRCR register.
(2) The START bit of the IRRCR register is set to "1" to start infrared remote control and infrared signal reception
(3) To enable an interrupt at the time of receiving a frame of the signal, the IRRIF bit is set to "1."
(4) To enable an interrupt at the time of transmitting a frame of the signal, the TDIE bit is set to "1."

[For infrared signal reception]

(1) When a frame of data has been received (RDI=1), the IRRIF bit of the RTKISR register is set to "1."
(2) When an interrupt at completion of signal reception has been enabled (RDIE=1), an interrupt occurs when a frame of data is stored in the IRRRFDE register.
(3) To obtain the received data, the receiving FIFO data register (IRRRFDR) is read. The IRRRFDR register contains a data count (that indicates the number of items of one frame of data received) and the received data itself. If this register is read, the data count and data itself are output in this order.
(4) The size of received data is set in the received data count register (IRRRDNR). When two frames have been received, the total data count and the two frames of data are set in the received data count register (IRRRDNR).

[For infrared signal transmission]

(1) When transmission data is transmitted, it is written to the transmitting FIFO data register. The data count for one frame of transmission data and the data itself are written to this data register. In addition, this transmission data count is not counted as transmission data.
(2) The count for data not transmitted is set in the transmission data count register (IRRSDNR).
(3) Data can be written to the transmission data IRRSFDR until the count for data not transmitted (IRRSDNR) reaches 255.
(4) When a frame of data has been transmitted (TDI=1), the IRRIF bit of the RTKISR register is set to "1." An interrupt for transmission completion occurs so long as it is enabled.

[Notes]

(1) To change the type of format, the FORMAT value of the same register must be set before the START bit of the IRRCR register is set to "1."
(2) When the START bit of the IRRCR register is "0," transmission/reception is not guaranteed.
(3) When the specified size is larger than the IRRRDNR value during a read operation, "FF" is set for excessive read data.
(4) Only the custom code and data code are specified for transmission data, and the leader, stop bit, frame space, and trailer are automatically added.
(5) When the number of write data items is larger than that of the remaining transmission data (255–byte transmission data count register IRRSDNR), a data length error occurs.
(6) When the IRRFDR register has become full during a read operation, the buffer full error bit is set to "1," and the data received later is discarded.
(7) The RIRRIF bit of the TKISR register is cleared when "0" is written with the IRRIF bit set to "1."

6.11 Serial EEPROM Control

This section describes the EEPROM control functions. Table 6.11 summarizes the serial EEPROM control registers. For details of each register, refer to 6.11.1 to 6.11.3.

(1) Serial EEPROM (512 bytes) can be read and written.

Table 6.11 Serial EEPROM Control Registers

Register	Abbreviation	Address	R/W	Size
EEPROMcontrol register	EEPCR	0x00C0	R/W	1 byte
EEPROM status register	EEPSR	0x00C1	R/W	1 byte
EEPROM data register	EEPDR	0x0100~0x02FF	R/W	1 byte x 512

6.11.1 EEPROM Control Register (EEPCR)

Address: 0x00C0 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	START
R	R	R	R	R	R	R	R/W

(1) START

START bit	Setting
0	The serial EEPROM is disabled. (Initial value)
1	The serial EEPROM is enabled.

6.11.2 EEPROM Status Register (EEPSR)

Address: 0x00C1 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	EEPWER
R	R	R	R	R	R	R	R

(1) EEPWER

EEPWER bit	Setting
0	No error has occurred during an EEPROM write operation. (Initial value)
1	An error has occurred during an EEPROM write operation.

6.11.3 EEPROM Data Register (EEPDR)

Address: 0x0100 to 0x02FF Initial value: Not defined

D7	D6	D5	D4	D3	D2	D1	D0
EEPDR_D7	EEPDR_D6	EEPDR_D5	EEPDR_D4	EEPDR_D3	EEPDR_D2	EEPDR_D1	EEPDR_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register consists of 512 8-bit data in the above format.

EEPDR address	
0x0100	8 bit
0x0101	8 bit
	•
	•
	•
0x02FE	8 bit
0x02FF	8 bit

An EEPROM address corresponds to an EEPDR address. When a read/write operation is performed on the EEPROM, the EEPDR address must be specified for the operation.

6.11.4 Serial EEPROM Operation Procedure

[Initial Setting]

(1) The START bit of the EEPGR register is set to “1.”

[For a read/write operation to the serial EEPROM]

(1) An EEPDR address corresponding to an EEPROM address must be specified for a read/write operation.

[Note]

(1) When the START bit of the EEPGR register is “0,” read/write data is not guaranteed.

6.12 Electronic Volume Control

This section describes the electronic volume control functions. Table 6.12 summarizes the electronic volume control registers. For details of each register, refer to 6.12.1 and 6.12.2.

(1) An electronic volume value can be set.

An electronic volume value can be set within a range from 0x00 (minimum sound volume) to 0xFF (maximum sound volume).

(2) Two electronic volume values can be set.

An electronic volume value can be set for the right or left speaker.

Table 6.12 Electronic Volume Control Registers

Register	Abbreviation	Address	R/W	Size
Electronic volume data register for the right speaker	EVRDR	0x00D0	R/W	1 byte
Electronic volume data register for the left speaker	EVLDR	0x00D1	R/W	1 byte

6.12.1 Electronic Volume Data Register for the Right Speaker (EVRDR)

Address: 0x00D0 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
EVRDR_D7	EVRDR_D6	EVRDR_D5	EVRDR_D4	EVRDR_D3	EVRDR_D2	EVRDR_D1	EVRDR_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Values from 0x00 to 0xFF can be set.

6.12.2 Electronic Volume Data Register for the Left Speaker (EVLDR)

Address: 0x00D1 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
EVLRD_D7	EVLRD_D6	EVLDR_D5	EVLDR_D4	EVLDR_D3	EVLDR_D2	EVLDR_D1	EVLDR_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Values from 0x00 to 0xFF can be set.

6.13 Power Supply Controller Initial Values

The register values for the power supply controller vary depending on the following conditions. Under condition A, all the power supply controller registers are initialized. The initial value of each register is given in the description of each register in this manual.

For register values under conditions A to D, refer to the following table of RTC registers.

[Condition]

Condition A: The power is turned ON.

The hard reset switch (SW4) is pressed.

Condition B: The power is turned OFF.

The RESTCR SORES bit has been set to "1."

The RESTCR SWRES bit has been set to "1," and the reset switch (SW2) has been pressed.

Condition C: The RESTCR SWES bit has been cleared to zero and the reset switch (SW2) has been pressed.

Condition D: The SPOWCR1 SPOWER bit has been set to "0."

Table 6.13 Values under RTC Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
RTC control register	RTCCR	Initial value	Initial value	Hold	Initial value
RTC status register	RTCSR	Initial value	Hold	Hold	Hold
Second counter	SECCNT	Initial value	Operation	Operation	Operation
Minute counter	MINCNT	Initial value	Operation	Operation	Operation
Hour counter	HRCNT	Initial value	Operation	Operation	Operation
Day-of-the-week counter	WKCNT	Initial value	Operation	Operation	Operation
Day counter	DAYCNT	Initial value	Operation	Operation	Operation
Month counter	MONCNT	Initial value	Operation	Operation	Operation
Year counter	YRCNT	Initial value	Operation	Operation	Operation
Second alarm counter	SECAR	Initial value	Hold	Hold	Hold
Minute alarm counter	MINAR	Initial value	Hold	Hold	Hold
Hour alarm counter	HRAR	Initial value	Hold	Hold	Hold
Day-of-the-week alarm counter	WKAR	Initial value	Hold	Hold	Hold
Day alarm counter	DAYAR	Initial value	Hold	Hold	Hold
Month alarm counter	MONAR	Initial value	Hold	Hold	Hold
RTC/Touch Panel/Key Input/Power Supply status register	RTKISR	Initial value	Initial value	Hold	Initial value

Table 6.14 Values under Touch Panel Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
Touch panel control register	TPLCR	Initial value	Initial value	Hold	Initial value
Touch panel status register	TPLSR	Initial value	Initial value	Hold	Initial value
Touch panel sampling control register	TPLSCR	Initial value	Initial value	Hold	Initial value
X position A/D register	XPAR	Initial value	Initial value	Hold	Initial value
Y position A/D register	YPAR	Initial value	Initial value	Hold	Initial value
X position dot register	XPDR	Initial value	Initial value	Hold	Initial value
Y position dot register	YPDR	Initial value	Initial value	Hold	Initial value
XA position dot register	XAPDR	Initial value	Hold	Hold	Hold
YA position dot register	YAPDR	Initial value	Hold	Hold	Hold
XB position dot register	XBPDR	Initial value	Hold	Hold	Hold
YB position dot register	YBPDR	Initial value	Hold	Hold	Hold
XC position dot register	XCPDR	Initial value	Hold	Hold	Hold
YC position dot register	YCPDR	Initial value	Hold	Hold	Hold
XA position A/D register	XAPAR	Initial value	Hold	Hold	Hold
YA position A/D register	YAPAR	Initial value	Hold	Hold	Hold
XB position A/D register	XBPAR	Initial value	Hold	Hold	Hold
YB position A/D register	YBPAR	Initial value	Hold	Hold	Hold
XC position A/D register	XCPAR	Initial value	Hold	Hold	Hold
YC position A/D register	YCPAR	Initial value	Hold	Hold	Hold
DX dot register	DXDR	Initial value	Hold	Hold	Hold
DY dot register	DYDR	Initial value	Hold	Hold	Hold
X position dot calculation A/D value	XPARDOT	Initial value	Hold	Hold	Hold
X position dot calculation A/D value 1	XPARDOT1	Initial value	Hold	Hold	Hold
X position dot calculation A/D value 2	XPARDOT2	Initial value	Hold	Hold	Hold
X position dot calculation A/D value 3	XPARDOT3	Initial value	Hold	Hold	Hold
X position dot calculation A/D value 4	XPARDOT4	Initial value	Hold	Hold	Hold
Y position dot calculation A/D value	YPARDOT	Initial value	Hold	Hold	Hold
Y position dot calculation A/D value 1	YPARDOT1	Initial value	Hold	Hold	Hold
Y position dot calculation A/D value 2	YPARDOT2	Initial value	Hold	Hold	Hold
Y position dot calculation A/D value 3	YPARDOT3	Initial value	Hold	Hold	Hold
Y position dot calculation A/D value 4	YPARDOT4	Initial value	Hold	Hold	Hold
RTC/Touch Panel/Key Input/Power Supply status register	RTKISR	Initial value	Initial value	Hold	Initial value

Table 6.15 Values under Switch Input Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
Key controle register	KEYCR	Initial value	Initial value	Hold	Initial value
Key auto repeat register	KATIMER	Initial value	Initial value	Hold	Initial value
Key input status register	KEYSR	Initial value	Initial value	Hold	Initial value
Key bit pattern register	KBITPR	Initial value	Initial value	Hold	Initial value
RTC/Touch Panel/Key Input/Power Supply status register	RTKISR	Initial value	Initial value	Hold	Initial value

Table 6.16 Values under Power Supply Control Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
System power control register 1	SPOWCR1	Initial value	Initial value	Hold	0x00
System power control register 2	SPOWCR2	Initial value	Initial value	Hold	Initial value
RTC/Touch Panel/Key Input/Power Supply status register	RTKISR	Initial value	Initial value	Hold	Initial value

Table 6.17 Values under LED Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
LED register	LEDR	Initial value	Initial value	Hold	0x00

Table 6.18 Values under LCD Front Light Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
LCD front light register	LCDR	Initial value	Initial value	Hold	0x00

Table 6.19 Values under Reset Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
Reset control register	RESTCR	Initial value	Initial value	Hold	Initial value

Table 6.20 Values under Infrared Remote Control Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
Infrared remote control register	IRRCR	Initial value	Initial value	Hold	Initial value
Infrared remote control status register	IRRSR	Initial value	Initial value	Hold	Initial value
Receive data count register for infrared remote control signals	IRRRDNR	Initial value	Initial value	Hold	Initial value
Transmit data count register for infrared remote control signals	IRRSDNR	Initial value	Initial value	Hold	Initial value
Receiving FIFO data register for infrared remote control signals	IRRRFDR	Initial value	Initial value	Hold	Initial value
Transmitting FIFO data register for infrared remote control signals	IRRSFDR	Initial value	Initial value	Hold	Initial value

Table 6.21 Values under Serial EEPROM Control Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
EEPROM control register	EEPCR	Initial value	Initial value	Hold	Initial value
EEPROM status register	EEPSR	Initial value	Initial value	Hold	Initial value
EEPROM data register	EEPDR	Initial value	Initial value	Hold	Initial value

Table 6.22 Values under Electronic Volume Control Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
Electronic volume data register for the right speaker	EVRDR	Initial value	Initial value	Hold	Initial value
Electronic volume data register for the left speaker	EVLDR	Initial value	Initial value	Hold	Initial value

7. Eeternal Interrupt

7.1 SH7760 External Interrupts

Figure 7.1 shows a mechanism for the SH7760 interrupt signal.

Table 7.1 shows the levels for respective interrupt signals.

As shown in Figure 7.1, interrupt signals from devices within Solution Engine2 are converted into the /IRL signals by FPG, then output to the /IRL [3:0] of the SH7760.

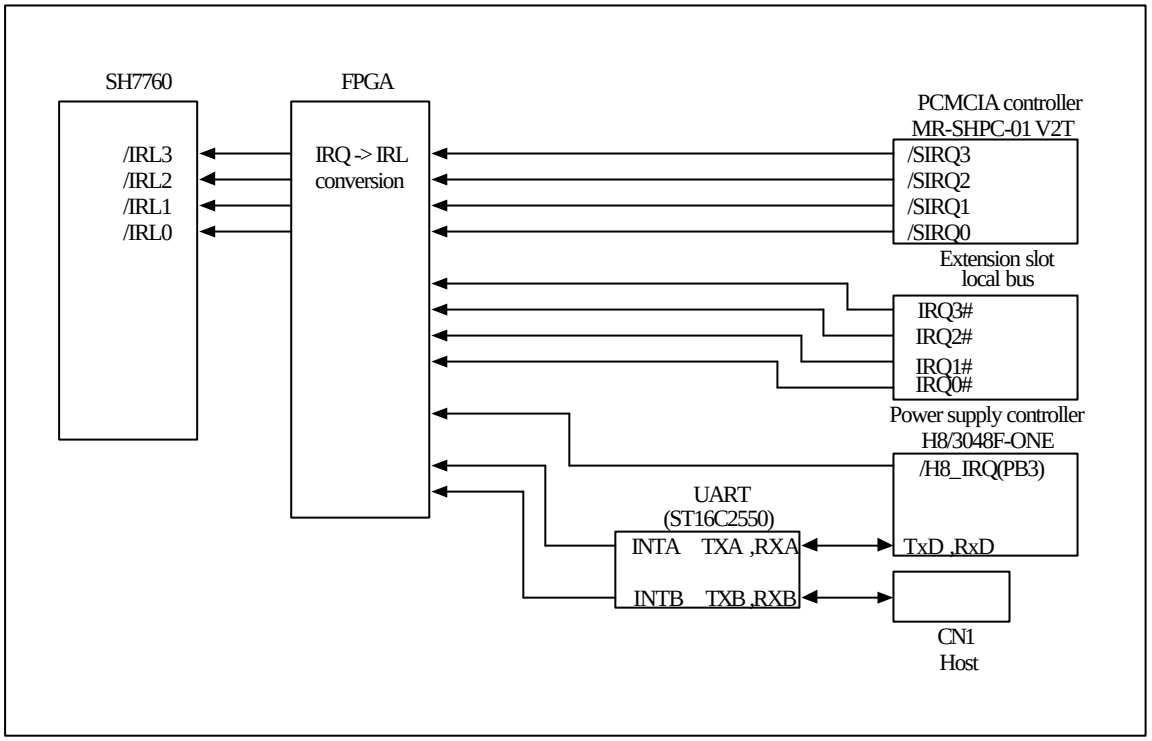


Figure 7.1 InterruptSignal Mechanism

Table 7.1 Interrupt Levels for Interrpt Signals

No	Interrupt request source	Interrupt input pin	Interrupt signal level	Remarks
1	PCMCIA controller (SIRQ3)	/IRL[3:0]	/IRL[3:0]=0001	Interrupt level 14
2	PCMCIA controller (SIRQ2)	/IRL[3:0]	/IRL[3:0]=0101	Interrupt level 10
3	PCMCIA controller (SIRQ1)	/IRL[3:0]	/IRL[3:0]=1000	Interrupt level 7
4	PCMCIA controller (SIRQ0)	/IRL[3:0]	/IRL[3:0]=1010	Interrupt level 5
5	UART controller chA	/IRL[3:0]	/IRL[3:0]=0110	Interrupt level 9
6	UART controller chB	/IRL[3:0]	/IRL[3:0]=0011	Interrupt level 12
7	H8/3048F-ONE	/IRL[3:0]	/IRL[3:0]=0010	Interrupt level 13
8	Extension slot (IRQ3#)	/IRL[3:0]	/IRL[3:0]=0000	Interrupt level 15
9	Extension slot (IRQ2#)	/IRL[3:0]	/IRL[3:0]=0100	Interrupt level 11
10	Extension slot (IRQ1#)	/IRL[3:0]	/IRL[3:0]=0111	Interrupt level 8
11	Extension slot (IRQ0#)	/IRL[3:0]	/IRL[3:0]=1001	Interrupt level 6

8. Solution Engine 2 Extension Slot

8.1 Extension Slot Specifications

Connector number: CN2

Solution Engine2 connector model: 20-5603-14-0101-861 (Kyocera Elco)
Adaptable connector model: 10-5603-14-0101-861 (Kyocera Elco)

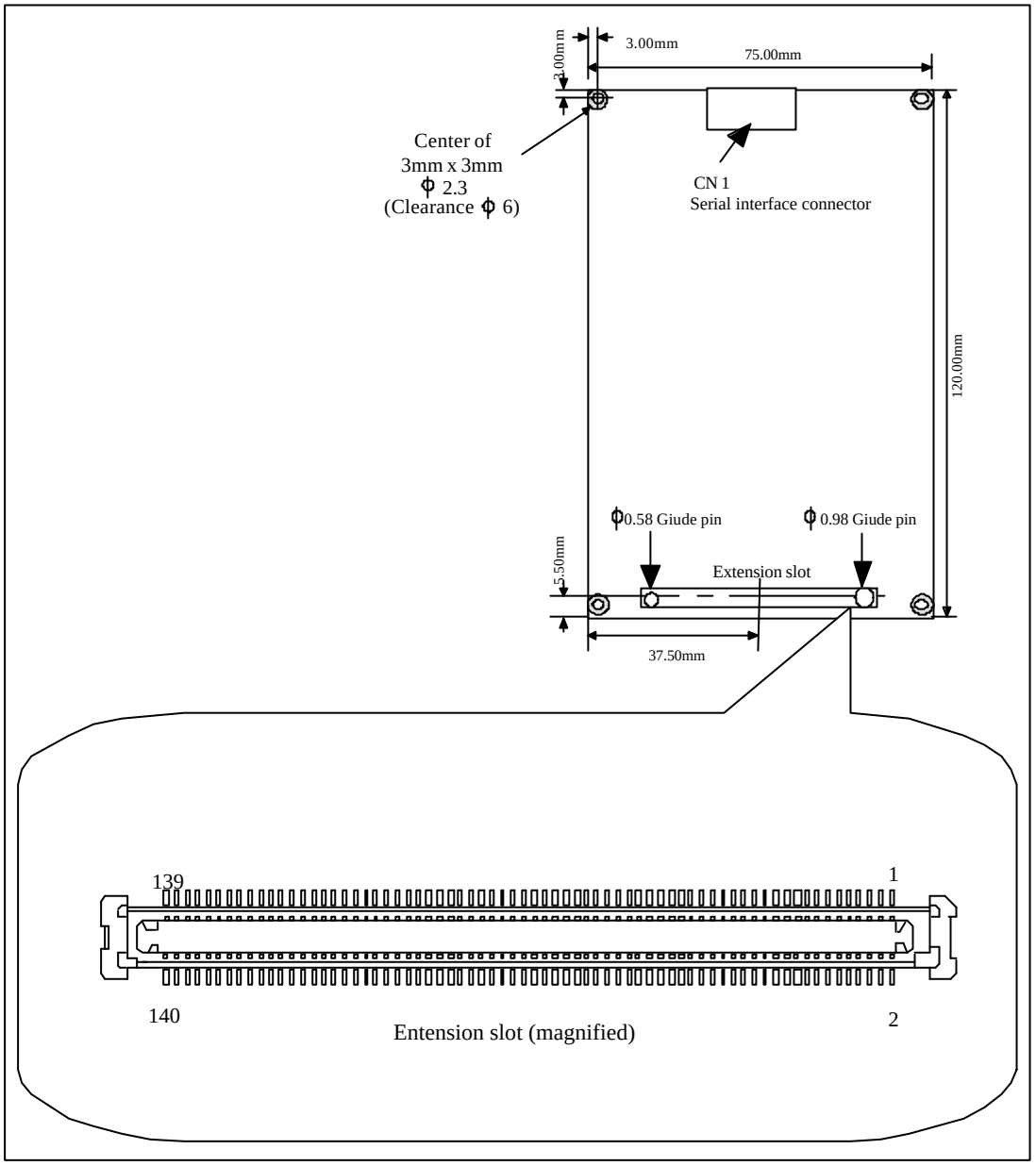


Figure 8.1 Extension Slot Position

8.2 Extension Slot Signal Assignment

Table 8.1 shows the assignment of extension slot signals.

Table 8.1 Extension Slot Signal Assignment

Pin No.	Signal name	I/O	Pin No.	Signal name	I/O	Pin No.	Signal name	I/O	Pin No.	Signal name	I/O
1	5V (*1)	-	36	D29	I/O	71	A24	OUT	106	SCIF2_CTS#	IN
2	5V	-	37	D30	I/O	72	A25	OUT	107	-	-
3	5V	-	38	D31	I/O	73	EPROMCE#	OUT	108	-	-
4	5V	-	39	GND	-	74	CS2#	OUT	109	GND	-
5	D0	I/O	40	GND	-	75	CS4#	OUT	110	GND	-
6	D1	I/O	41	CKIO	OUT	76	CS5#	OUT	111	TCK	IN
7	D2	I/O	42	GND	-	77	RDWR	OUT	112	TMS	IN
8	D3	I/O	43	GND	-	78	BS#	OUT	113	TRST#	IN
9	D4	I/O	44	GND	-	79	GND	-	114	TDI	IN
10	D5	I/O	45	A0	OUT	80	GND	-	115	TDO	OUT
11	D6	I/O	46	A1	OUT	81	RD#	OUT	116	ASEBRKAK#	OUT
12	D7	I/O	47	A2	OUT	82	WAIT#	IN	117	3.3VSB (*3)	-
13	D8	I/O	48	A3	OUT	83	WE0#	OUT	118	3.3VSB	-
14	D9	I/O	49	A4	OUT	84	WE1#	OUT	119	3.3VSB	-
15	D10	I/O	50	A5	OUT	85	WE2#	OUT	120	3.3VSB	-
16	D11	I/O	51	A6	OUT	86	WE3#	OUT	121	AUDATA0	I/O
17	D12	I/O	52	A7	OUT	87	GND	-	122	AUDATA1	I/O
18	D13	I/O	53	A8	OUT	88	GND	-	123	AUDATA2	I/O
19	D14	I/O	54	A9	OUT	89	IRQ0#	IN	124	AUDATA3	I/O
20	D15	I/O	55	A10	OUT	90	IRQ1#	IN	125	AUDSYNC#	OUT
21	GND	-	56	A11	OUT	91	IRQ2#	IN	126	AUDCK	IN
22	GND	-	57	A12	OUT	92	IRQ3#	IN	127	3.3V (*4)	-
23	D16	I/O	58	A13	OUT	93	NMI_IN	IN	128	3.3V	-
24	D17	I/O	59	A14	OUT	94	RST_IN#	IN	129	3.3V	-
25	D18	I/O	60	A15	OUT	95	RST_OUT#	OUT	130	3.3V	-
26	D19	I/O	61	GND	-	96	DREQ#	IN	131	3.3V	-
27	D20	I/O	62	GND	-	97	DRAK#	OUT	132	3.3V	-
28	D21	I/O	63	A16	OUT	98	DACK#	OUT	133	VBAT_IN (*5)	-
29	D22	I/O	64	A17	OUT	99	ROMSEL	IN	134	VBAT_IN	-
30	D23	I/O	65	A18	OUT	100	BASE# (*2)	IN	135	VBAT_IN	-
31	D24	I/O	66	A19	OUT	101	GND	-	136	VBAT_IN	-
32	D25	I/O	67	A20	OUT	102	GND	-	137	GND	-
33	D26	I/O	68	A21	OUT	103	SCIF2_TXD	OUT	138	GND	-
34	D27	I/O	69	A22	OUT	104	SCIF2_RXD	IN	139	GND	-
35	D28	I/O	70	A23	OUT	105	SCIF2_RTS#	OUT	140	GND	-

: Indicates the SH7760 address bus, data bus, control signal, and serial signal. The supply voltage is 3.3V.

*1: 5.0V (typ.) is supplied when the SH7760 is turned ON.

*2: When this pin is set to “Low,” output is made from the SH7760 extension bus to the extension slot.

*3: When a battery has been connected and an AC adapter is connected, 3.3V (typ.) is always supplied.

*4: When the SH7760 is turned ON, 3.3V (typ.) is supplied.

*5: Power supply pin (4.2V to 3.6V). This voltage is applied to Solution Engine2 via the extension slot.

9. Daughter Board Design Guide

This chapter describes the design of the daughter board to be connected to the extension slot of Solution Engine2. The daughter board may contain user-specific devices and can be controlled by the address bus, data bus, and control signals of the SH7760 that connect to the extension slots of Solution Engine2.

9.1 Daughter Board Dimensions

The recommended daughter board size is the CPU board size (120mm x 75mm) of Solution Engine2.

9.2 Daughter Board Power Supply

Table 9.1 shows the voltage and current that can be supplied from Solution Engine2 to a daughter board. When a daughter board requires more current, a power supply must be mounted on the daughter board.

Table 9.1 Voltage and Current to the Daughter Board

Extension slot signal name	Output voltage	Permissible current	Remarks
3.3V 3.3VSB	3.3V	250mA	3.3V: Supplied when the H7760 is turned ON. 3.3VSB: Always supplied when the AC adais connected.
5V	5V	250mA	Supplied when the SH4460 is turned ON.

[Note]

(1) When a peripheral device operating on the bus power via the USB has been connected to Solution Engine2 or the PCMCIA card is in use, the permissible current is the current obtained by subtracting the dissipation current of the device and card from the permissible current.

9.3 Daughter Board Stack

A maximum of 3 daughter boards can be stacked. When multiple daughter boards are stacked, care should be taken for electric capacity. Figure 9.2 shows an example of daughter board stacks.

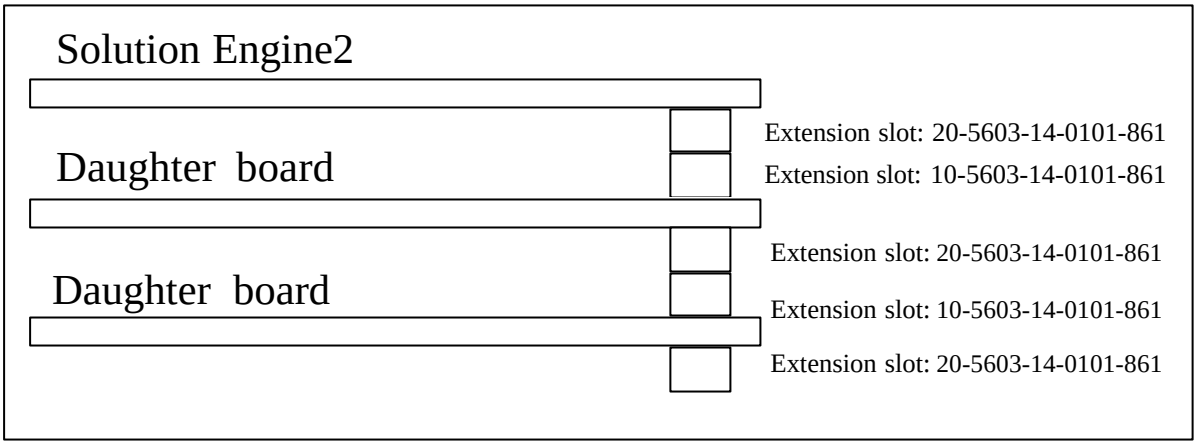


Figure 9.2 Daughter Board Stack

9.4 Daughter Board WAIT# Output

Solution Engine2 is provided with a WAIT# input pin on the extension slot for WAIT input to the daughter board. When a WAIT# is output from the daughter board, open collector output must take place to prevent a collision of WAIT# output when multiple daughter boards are stacked.

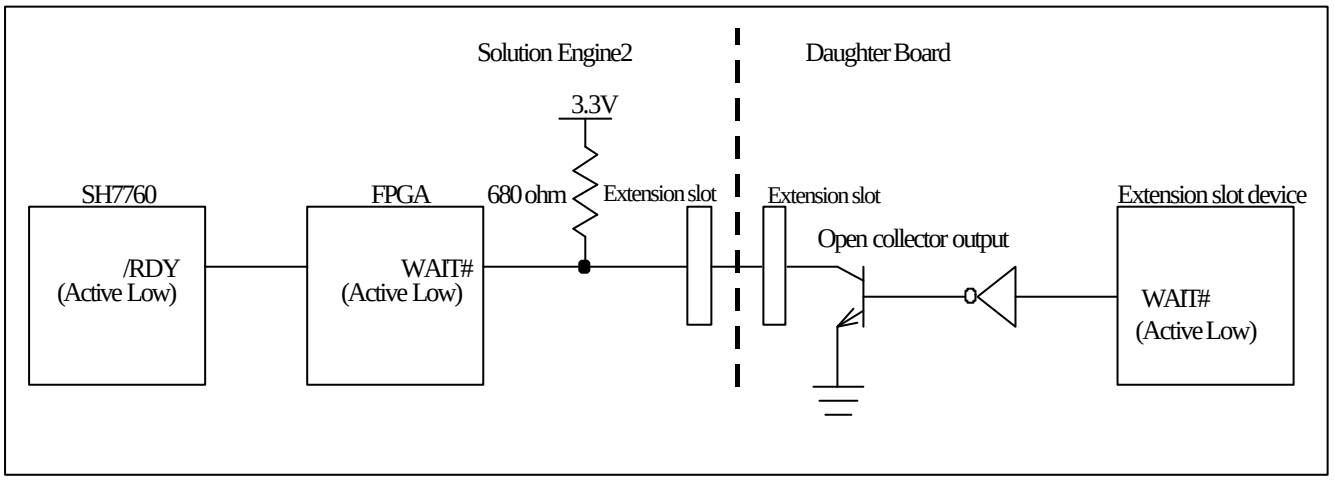


Figure 9.3 Extension Slot IORDY Pin Structure

9.5 Extension Slot AC Timing

As shown in Figure 9.4, the SH7760 bus signal is output to the extension slot via the bus buffer. For this reason, the bus signal delays approx. 8nsec for the AC timing of the SH7660 bus. When designing the daughter board, consider this delay. Figure 9.5 shows the basic bus timing of the SH7760.

For details on SH7760 bus timing, refer to the pertinent SH7760 Hardware Manual.

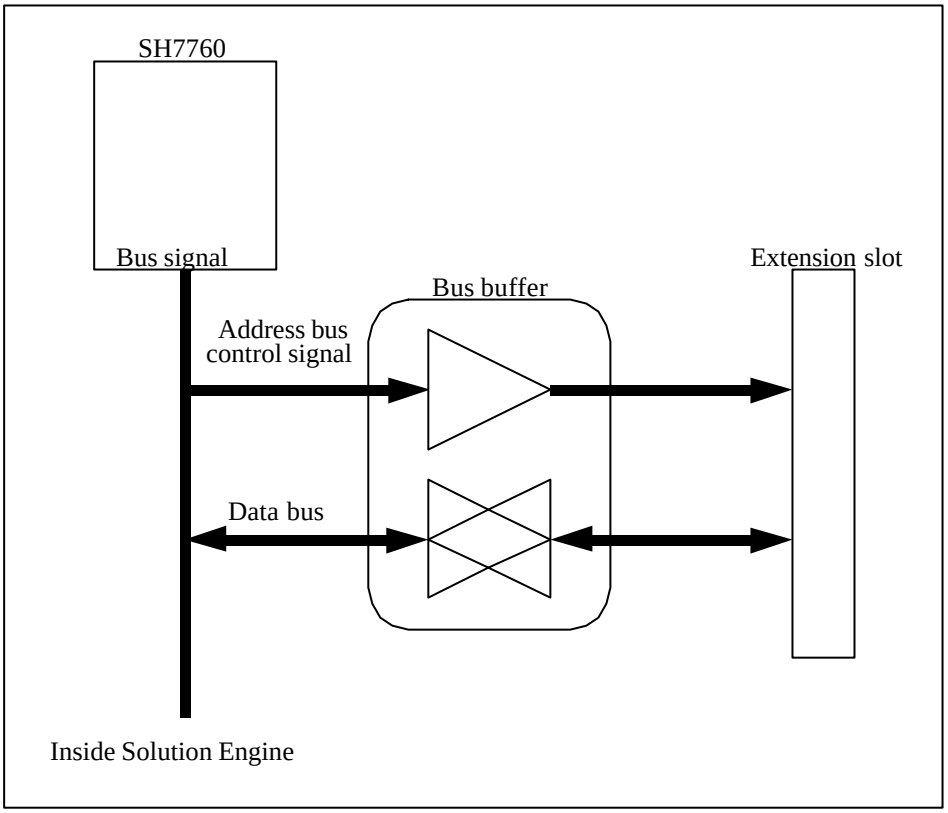
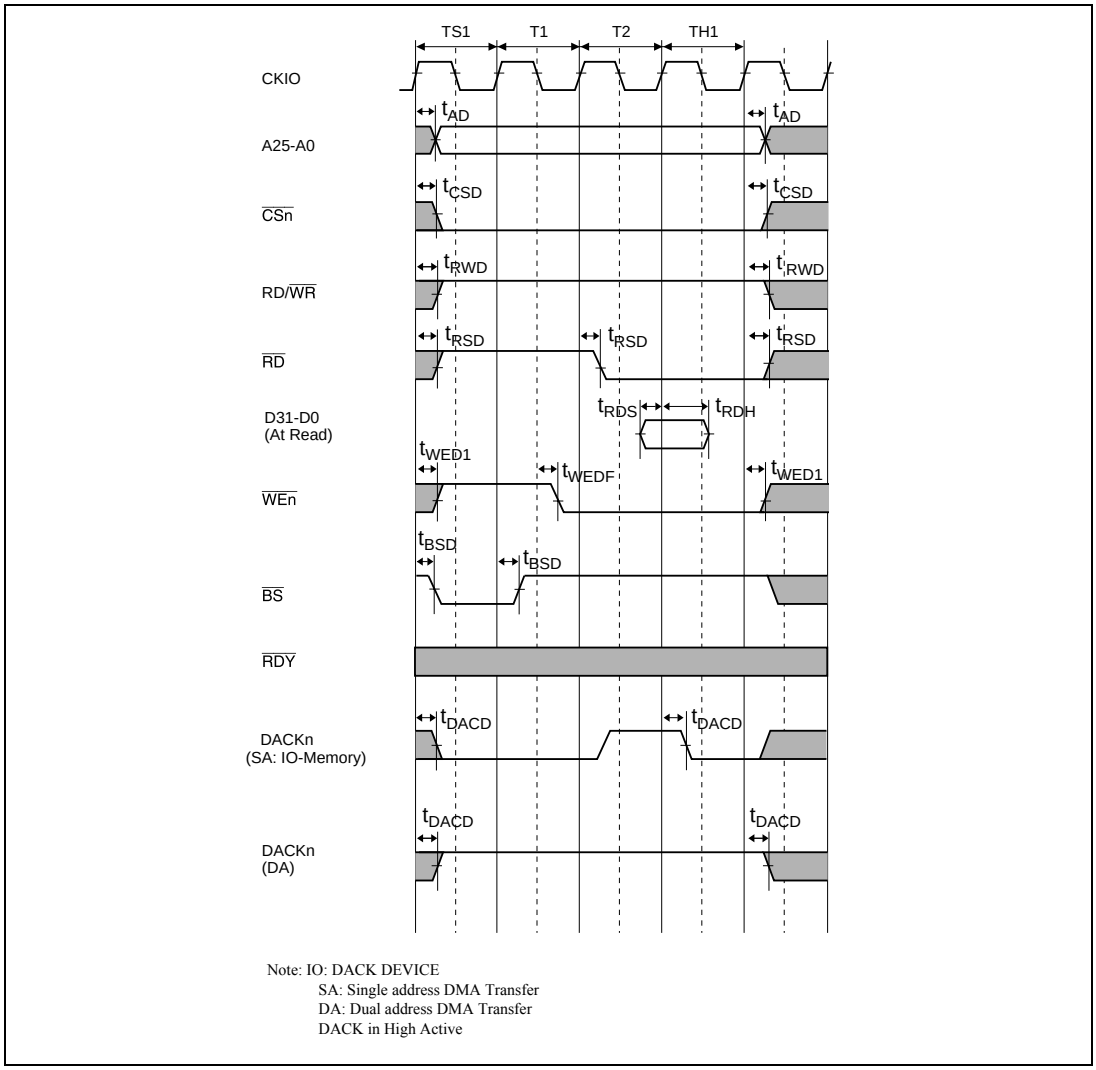


Figure 9.4 Extension Slot Bus Buffer Structure

[Note]

(1) The bus timing delay time must be used only for reference. This is not a guaranteed value.



Note: IO: DACK DEVICE
SA: Single address DMA Transfer
DA: Dual address DMA Transfer
DACK in High Active

Figure9.5 Memory Byte control SRAM Bus cycle Basic Read cycle
(No wait, Address set up/Insert hold time, AnS=1, AnH=1)

10. Monitor Program Usage

10.1 Monitor Program Usage

(1) Host system connection

Connect the host system serial port to the Solution Engine2 CN1 with an accessory RS-232C cross cable. When serial connection is complete, start communication software (HyperTerminal or Windows terminal. Make communication settings as shown in Table 12.1. In addition, this monitor program outputs CR+LF as a carriage return code.

Table 10.1 Communication Specifications

Data length	8 bit
Parity bit	None
Stop bit	1 bit
Baud rate	115200bps
Flow control	Xon/Xoff

(2) Monitor program specifications

Figure 10.1 shows a monitor program address map. Don't write to the area used by the monitor program (h'0FFF0000 to h'0FFFFFF). For details of each memory area, refer to 4, "Memory Map."

h’00000000 ~ h’003FFFFF	EPROM area monitor program	CS0 area (bus width: 16bit)
h’00400000 ~ h’007FFFFF	Debug LED area	
h’00800000 ~ h’00BFFFFF	Switch area	
h’00C00000 ~ h’00FFFFFF	Unused area	
h’01000000 ~ h’01FFFFFF	Flash memory area	
h’02000000 ~ h’03FFFFFF	Unused area	
h’04000000 ~ h’07FFFFFF	Board control register area	CS1 area (bus width: 16bit)
h’08000000 ~ h’0BFFFFFF	Extension area (CS2)	CS2 area (bus width: arbitrary)
h’0C000000 ~ h’0FFEFFFF	User area	CS3 area SDRAM area (bus width: 32bit)
h’0FFF0000 ~ h’0FFFFFFF	Area used by the monitor program	
h’10000000 ~ h’13FFFFFF	Extension area (CS4)	CS4 area (bus width: arbitrary)
h’14000000 ~ h’17FFFFFF	Extension area (CS5)	CS5 area (bus width: arbitrary)
h’18000000 ~ h’1BFFFFFF	PCMCIA area	CS6 area (bus width: 16bit)

Figure 10.1 Memory Map (Real Memory Space)

(3) Monitor program start

Connect Solution Engine2 and the host system with an RS-232C cross cable. When the monitor program starts, the following starting message appears on the host system screen.

```
================================================
     SH7760 Self Debugger     Ver  x.xL  (****/**/**)
 ------------------------------------------------------------------------
     (C) Copyright 2002-2005.  Hitachi.Ltd. All rights reserved.
================================================
    Ready >                                  H [elp] for help messages...
```

In the above starting message, a version number is displayed in xx.

(4) User program download

When a user program is downloaded into the user RAM, use the ml command. As shown below, enter “ml” at the command prompt.

```
Ready > ml
```

After command entry, the following transfer request message is output from the monitor program, and the message is displayed on the host system screen.

```
Please Send A S-format Record
```

When the above message is displayed, send the S format object file by using the file transfer function of the communication software.

The S format object file has been provided with address information, and the object program is located according to this information.

When the object file has no address information, i.e., it is a relocatable file, specify an offset address with the ml command.

This offset address must be within a user area shown in Figure 10.1. Upon completion of file loading into memory, the following message is displayed on the screen of the host system. (In this example, the program has been loaded from the address h’AC100000 in area 3.)

```
Ready >ml
Please Send A S-format Record

 Start Addrs = AC100000
End Addrs = AC1000BC

 Transfer complete
  Ready >
```

(5) Display and change of register data

Before executing a program, set a stack point for the program loaded into memory in R15. Because R15 is already set to h'AFFF0000,' make the following change if the stack pointer is to be placed in a different location.

```
Ready >RW R15 AFC00000
```

When register setting is complete, the monitor program displays information on all the registers and enters a command prompt (command entry wait status).

```
Ready >RW R15 AFC00000
--General Registers-----------------------------------------------------------------------------------------
  R0-7   00000000  00000000  00000000  00000000  00000000  00000000  00000000  00000000
  R8-15 00000000  00000000  00000000  00000000  00000000  00000000  00000000  AFC00000
--Bank Registers-------------------------------------------------------------------------------------------
  R0-7   00000000  00000000  00000000  00000000  00000000  00000000  00000000  00000000
--Control Registers----------------------------------------------------------------------------------------
    SR = 60000090  SSR=60000090  SPC=00000000  GBR=00000000
    VBR= 00000000  SGR=00000000  DBR=00000000
    MD=  1  RB=1  BL=0  FD=0  M=0  Q=0  IMASK=0x9  S=0  T=0
 --System  Registers---------------------------------------------------------------------------------------
   PC = 0C000000  PR =00000000  MACH=00000000  MACL=00000000
    FPSCR= 00040001  FPUL=00000000
   FR= 0  SZ=0  PR=0  DN=1  Cause=0x00  Enable=0x00  Flag=0x00  RM=0x1
 --FPU Registers--------------------------------------------------------------------------------------------
    FR0-7   00000000  00000000  00000000  00000000  00000000  00000000  00000000  00000000
   FR8-15  00000000  00000000  00000000  00000000  00000000  00000000  00000000  00000000
    XF0-7  00000000  00000000  00000000  00000000  00000000  00000000  00000000  00000000
   XF8-15 00000000  00000000  00000000  00000000  00000000  00000000  00000000  00000000
    Ready >
```

(6) Memory data dump

Enter the ml command to check the program transferred to the user memory. This ml command must be entered as shown below.

```
Ready >MD AC000000
```

Once the ml command is executed, the contents of a 256-byte area (for example, h'AC000000 to h'A00000FF) are dumped.

```
Ready >MD AC000000
<ADDRESS>                    <  DATA  >
AC000000   EE 57 E7 D7 C1 BC 75 F6   5E F5 43 FA BB FF 2F 7F
AC000010   63 F3 64 DF 47 DD 15 F7   FF EF E7 F6 FF  FF D4 A4
AC000020   22 FC 01 7D C2 F7 33 BF   FF  FF FC D6 FF  FF DD F7
AC000030   F1 61 23 FD 0A E6 11 FF   B9 FF EE F3 FF FF B1 FF
AC000040   E6 89 12 FF 71 C9 63 9F   FD F7 FB EF FF A5 E7 BF
AC000050   6C 9C F7 98 67 7D 12 7E   FF  FF F9 EF FF  FF 7D F3
AC000060   A3 BC 77 EB 2E 63 0E FD   FF EF 9E 37 FF FF F3 FF
AC000070   03 7A F7 F9 8A AB 09 FB   FF FF F7 EE F7 DF 48 DF
AC000080   49 B9 80 FE FF FF 45 FF   FF F7 A8 F7 BC 9F BB F5
AC000090   EC E9 6A FB FF  FF FD E9  FF 7F AE E8 2A DB 2B BF
AC0000A0   B8 E1 35 5F DF FF FF  FF  DF FF 87 66 E3 97 F8 F9
AC0000B0   CD F4 7D 67 F1 6B BC E7   7F FF 3D FF 9D F7 3D FF
AC0000C0   4A FF B3 37 FF FF 27 BF   FF  FF D7 EE 79 33 9B 4F
AC0000D0   6A 05 31 FE FF DF 31 73   FF FF EF 47 2E C2 D2 6F
AC0000E0   4A 42 BB F8 F7 FF 6B FB  FB F5 DD 4F 19 A2 42 FB
AC0000F0   4A 4A 80 7F FF FF 76 FE   FE FB 6B 66 11 D7 3B E2
```

(7) User program execution

Use the g command to run the program transferred to the user memory. Enter this g command as shown below.

```
Ready >G AC000000
```

As shown above, the address h'AC000000 is set in the program counter (PC), and the program is run from that address. When Ctrl + C is input in the operation terminal (computer), the monitor program displays information on all the registers and interrupts the execution of user programs.

```
--General Registers----------------------------------------------------------------------------------------
  R0- 7 00000000   00000000 00000000 00000000 00000000 00000000   00000000 00000000
 R8-15 00000000   00000000 00000000 00000000 00000000 00000000   00000000 AFFF0000
--Bank Registers-------------------------------------------------------------------------------------------
  R0- 7 00000000   00000000 00000000   00000000 00000000 00000000   00000000 00000000

       SR =600000E1   SSR=60000090   SPC=AC00001C   GBR=00000000
     VBR=00000000   SGR=AFFF0000   DBR=00000000
       MD=1  RB=1  BL=0  FD=0  M=0  Q=0  IMASK=0xE  S=0  T=1
 --System  Registers---------------------------------------------------------------------------------------
      PC =AC00001C   PR =00000000  MACH=00000000  MACL=00000000
FPSCR= 00040001  FPUL=00000000
      FR= 0  SZ=0  PR=0  DN=1  Cause=0x00  Enable=0x00  Flag=0x00  RM=0x1
   Ready >
```

(8) User program execution in units of steps

Use the s command to run the program transferred to the user memory in units of steps. Enter the s command as shown below.

```
Ready >S AC000000
```

If the s command is executed, the monitor program displays the executed addresses and information on all the registers.

```
 Ready >S AC000000
 AC000000 0009 NOP
 --General Registers----------------------------------------------------------------------------------------

  R0-7 00000000   00000000 00000000   00000000 00000000 00000000   00000000   00000000
 R8-15 00000000   00000000 00000000   00000000 00000000   00000000 00000000   AFFF0000
 --Bank Registers-------------------------------------------------------------------------------------------
 R0- 7 00000000   00000000 00000000 00000000 00000000 00000000   00000000 00000000
 --Control Registers----------------------------------------------------------------------------------------
   SR =600000F0   SSR=60000090   SPC=AC000002   GBR=00000000
 VBR=00000000   SGR=AFFF0000   DBR=00000000
   MD=1  RB=1  BL=0  FD=0  M=0  Q=0  IMASK=0xF  S=0  T=0
 --System  Registers---------------------------------------------------------------------------------------
    PC = AC000002   PR =00000000  MACH=00000000  MACL=00000000
FPSCR=00040001  FPUL=00000000
     FR=0  SZ=0  PR=0  DN=1  Cause=0x00  Enable=0x00  Flag=0x00  RM=0x1
   Ready >
```

(9) Breakpoint setting

Use the bs command to set a breakpoint. Enter the bs command as shown below. If the bs command is entered as shown below, a breakpoint will be set at the address h'AC00000. If the monitor program is run in this state, a break will occur at that address and the user program will stop.

To make this break, an instruction at that address is replaced with an invalid instruction. For this reason, no break can be made for read-only memory like EPROM.

```
Ready >BS AC000010
Set Software Break Point CH 0=0xAC000010
```

To disable the set breakpoint, use the bi command.

```
Ready >BI
================
  < IGNORE BREAK >
================
PC Break Address
[0000] : AC000010
================
Ready >
```

To enable the set breakpoint disabled by the bi command, use the be command.

```
Ready >BE
================
< ENABLE BREAK >
================
 PC Break Address
 [0000] : AC000010
================
Ready >
```

(10) Change and display of memory data

Use the me command to change the contents of memory. Enter the me command as shown below. If characters other than hexadecimals are entered, the monitor program exits from the me command and displays the command prompt (command entry wait status).

```
Ready >ME AC000000
AC000000 09-
AC000001 00-.
Ready >
```

(11) Write to the flash memory

To transfer the user program to the user RAM and write it to the flash ROM, use the fl command. Enter “fl 0” at the command prompt. Before writing to the flash ROM, erase the flash ROM first. Figure 10.2 shows the procedure for writing the user program to the flash ROM and executing it from the flash memory. Specify “0” as an option for the fl command.

```
Ready >fl 0
```

After command entry, the monitor program displays the following transfer request message on the host system screen.

```
SH7760 Flash Memory Change Value!
Flash Memory data copy to RAM
Please Send A S-format Record
```

When this message appears, use the file transfer function of the communication software to send the S format object file.

The S format object file is provided with address information, and the object file is located according to this information.

When the object file has no address information, i.e., it is a relocatable file, specify an offset address in the fl command.

This offset address must be within a user area shown in Figure 12.1.

Upon completion of program loading into the memory, the following message is displayed on the host system screen. (In this example, the program has been loaded into the address h’A0000000 within area 3.)

```
Start  Addrs = A0000000
End  Addrs = A00FFFFF

Transfer complete
```

When flash ROM erasure begins, the monitor program displays the following message.

```
Flash chip erase: complete
Program :
```

Upon completion of ROM erasure, the monitor program begins to write to the flash ROM.

```
Flash chip erase:
```

When a write operation is complete, the monitor program displays the following command prompt on the screen.

```
Ready >fl 0

SH7760 Flash Memory Change Value!
Flash Memory data copy to RAM
Please Send A S-format Record

Start   Addrs = A0000000
End   Addrs = A00FFFFF

Transfer complete
Flash chip erase: complete
Program :complete
Flash write complete
Ready >
```

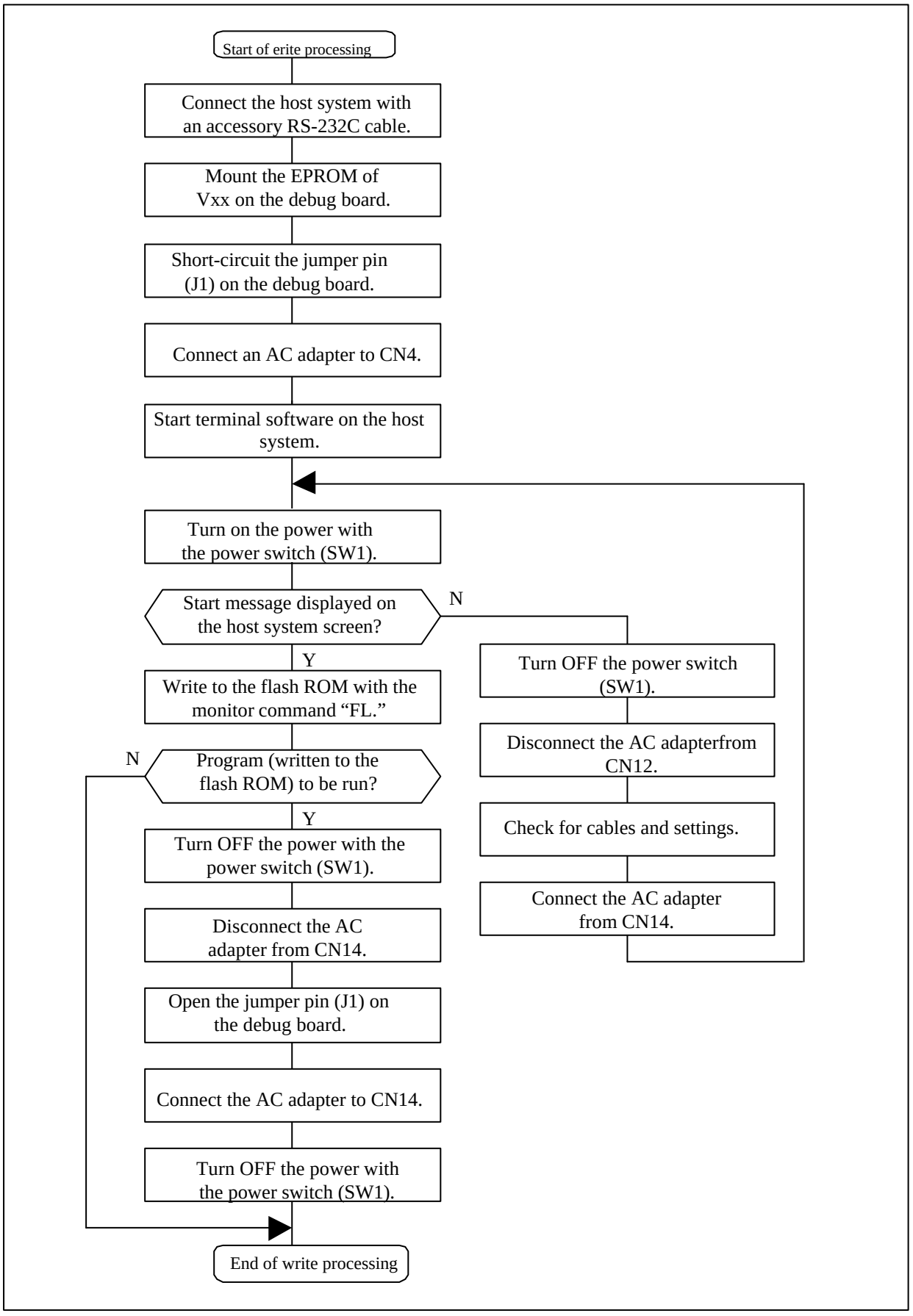


Figure 10.2 Procedure to write to Flash ROM

10.2 List of Monitor Program Functions

Table 10.2 summarizes the monitor program commands.

Table 10.2 List of Monitor Program Functions

Category	Command	Description
Host PC interface	ML (Memory Load)	Downloads an object from the host.
Write to the flash ROM	FL (Flash Load)	Writes to a flash ROM.
Register display	RR (Register Read)	Reads all the SH registers.
	RW (Register Write)	Writes to a specific SH register.
	RC (Register Clear)	Clears all the SH registers.
Memory	ME (Memory Edit)	Edits memory.
	MD (Memory Dump)	Dumps memory.
	MF (Memory Fill)	Fills memory.
	DA (Disassemble)	Disassemble
Program execution	G (Go)	Executes a program
	S (Step)	Executes a program in units of steps.
	BS (Breakpoint Set)	Sets a breakpoint.
	BD (Breakpoint Delete)	Deletes a breakpoint.
	BC (Breakpoint Clear)	Deletes all the breakpoints.
	BE (Break Enable)	Causes a break in a breakpoint.
	BI (Break Ignore)	Ignores a breakpoint.
Others	H (Help)	Gives a brief description of each command format.

10.3 Command Description

Command	Function
ML (Memory Load)	Loads an object from the host.
Option None	

Format

ML (offset address)

Example: Ready >ML
Ready >ML AC000000

(Note)
Though a program can be loaded by specifying an offset address, it is effective only when the program to be loaded does not depend on the absolute address. When a jump program using an absolute address is loaded with an offset address specified, its operation is not guaranteed. For this reason, don't specify an offset address and load the program into an address at linkage.

Command	Function
FL (Flash Load)	Writes data and programs into Flash ROM
Option	
"0" must be specified for a data/program transfer destination	

Format

FL 0

Example: Ready>FL

Write FL command to Flash ROM as follows.

(1) Make Flash ROM image on SDRAM

Make Flash ROM image on SDRAM by copying Flash ROM data to the first 8M-byte area of the SDRAM address

(2) Download S format object file

Transfer MOTOROLA S format object file on PC to SDRAM. MOTOROLA S format object files should be transferred to the following SDRAM address.

SDRAM address =MOTOROLA S format address + (SDRAM top address(H'0c000000))

Upper 4 bits of MOTOROLA S format address are ignored.

(3) Delete FlashROM data

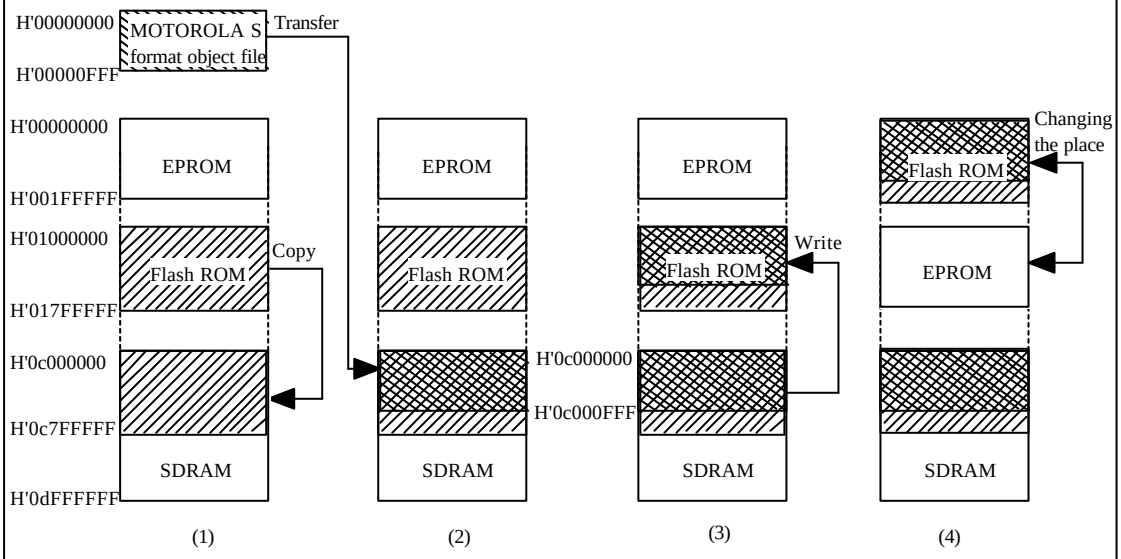
Delete all Flash ROM data after the transfer.

(4) Writing

Write first 8M-byte data of the SDRAM address to Flash ROM.

(5) Changing place between Flash ROM and EPROM

Change the place between EPROM and Flash ROM by DIP switch setting after writing. Programs written to Flash ROM can be run by changing the place.



Command	Function
RR (Register Lead)	Reads all the registers.
Option None	
Format RR	
Example: Ready >RR	

Command	Function
RW (Register Write)	Writes data to the corresponding register.
Option None	
Format RW <regname> <data>	
Example: Ready >RW R0 12AB	

Command	Function
RC (Register Clear)	Clears all registers with zeros.
Option None	
Format RC	
Example: Ready >RC	

Command	Function
ME (Memory Edit)	Edits Memory
Option	
-W,-L	Word access, log word access

Format

ME <address> (option)

Example: Ready >ME AC000000

Ready >ME AC000000 -W

Ready >ME AC000000 -L

Command	Function
MD (Memory Dump)	Dumps Memory
Option	
-A	Display in ASCII codes

Format

MD (start address) (end address)

Example: Ready >MD

Ready >MD 0

Ready >MD 0 200 -A

Command	Function
MF (Memory Fill)	Fills memory.
Option	
-(data)	Fill with specified data

Format

MF (start address) (end address) (option)

Example: Ready >MF

Ready >MF AC000000 AC000200

Ready >MF AC000000 AC000200 -55

Command	Function
DA (Disassemble)	Disassembles from a specified address.
Option None	
Format DA (start address)	
Example: Ready >DA AC000000	

Command	Function
G (Go)	Executes a program from a specified address.
Option None	
Format G (start address)	
Example: Ready >G AC000000	

Command	Function
S (Step)	Executes a program in units of steps from a specified address.
Option None	
Format S (start address)	
Example: Ready >S AC000000	

Command	Function
BD (Breakpoint Delete)	Disassembles from a specified address.
Option	
None	
Format	
BD <address>	
Example: Ready >BD 45C	

Command	Function
BS (Breakpoint Set)	Sets a breakpoint.
Option	
None	
Format	
BS (address)	
Example: Ready >BS AC000000	

Command	Function
BC (Break Clear)	Deletes all the breakpoints.
Option	
None	
Format	
BC	
Example: Ready >BC	

Command	Function
BI (Break Ignore)	Ignores a breakpoint.
Option	
None	
Format	
BI	
Example: Ready >BI	

Command	Function
BE (Break Enable)	Causes a break at a breakpoint.
Option	
None	
Format	
BE	
Example: Ready >BE	

Command	Function
H (Help)	Gives a description of the monitor system command.
Option	
(number)	Gives a description of the corresponding item.

Format

H (number)

Example:

```
Ready >H          <-- Displays a help menu.
-------------------------------------------------------------------------------------------
Debugger Help : Address or data must be specified by hex (need not H')
-------------------------------------------------------------------------------------------
[1] General          --- H
[2] Register         ---RC   RR   RW
[3] Break Point      ---BS   BR   BD   BC   BI   BE
[4] Memory           ---ML   ME   MD   MF   FL
[5] Disassemble      --- DA
[6] Start User Program ---G   S
[7] Cache            --- CA   CR   CE   CD   CF   CW   CB
.....H[elp] number(or class), for more information.
-------------------------------------------------------------------------------------------
Ready > H 4       <-- [4] Memory Detailed help display for memory-related commands
-------------------------------------------------------------------------------------------
Debugger    Help : [4] Memory
-------------------------------------------------------------------------------------------
Memory Load          : M[em]L[oad]
Memory Edit          : M[em]E[dit] startAdrs [size(-W,-L)]
Memory Dump          : M[em]D[ump] [startAdrs] [endAdrs] [ASCIIcode(-A)]
Memory Fill          : M[em]F[ill] [startAdrs] [endAdrs] [Data(-Data)]
Flash Load           : F[lash]L[oad] [offsetAdrs]
-------------------------------------------------------------------------------------------
Ready >
```

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